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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MINRUI YU, KAI MA, THOMAS KWON, KAUSHAL K. SINGH, and ER-XUAN PING

Appeal 2020-001876
Application 14/745,367
Technology Center 1700

Before LINDA M. GAUDETTE, N. WHITNEY WILSON, and BRIAN D. RANGE, *Administrative Patent Judges*.

WILSON, *Administrative Patent Judge.*

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's February 19, 2019 decision to finally reject claims 1, 4–6, 16–21, 23, 24, and 26–32 ("Final Act."). An oral hearing was held on September 24, 2020, a transcript of which will be part of the record. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Applied Materials Inc. (Appeal Br. 3).

CLAIMED SUBJECT MATTER

Appellant's Specification discloses a method for forming a film stack structure on a substrate (Abstract). In one embodiment, the method for forming a film stack structure on a substrate includes depositing a first adhesion layer on an oxide layer formed on the substrate and depositing a metal layer on the first adhesion layer, wherein the first adhesion layer and the metal layer form a stress neutral structure (*id.*). Claim 1, reproduced below from the Claim Appendix, is illustrative of the claimed subject matter:

> 1. A method for forming a film stack on a substrate, comprising:
>
> forming a plurality of oxide metal structures comprising sequential repetitions of:
>
> depositing an oxide layer using tetraethylorthosilicate (TEOS), the oxide layer having a first thickness of less than or equal to 250 Å;
>
> depositing an adhesion layer comprising tungsten nitride on the oxide layer; and
>
> depositing a metal layer comprising tungsten on the adhesion layer, wherein the adhesion layer and the metal layer form a stress neutral structure having a second thickness less than or equal to 200 Å, wherein each layer of the plurality of oxide metal structures is deposited using one of a plurality of processing chambers of a multi-chamber system, and wherein the plurality of oxide metal structures are sequentially formed before the substrate is removed from the multi-chamber system.

REFERENCES

The prior art relied upon by the Examiner is:

Name	Reference	Date
Miyanaga et al.	US 5,418,187	May 23, 1995
Mirkarimi et al.	US 6,011,646	January 4, 2000
Yamamoto	US 6,437,441 B1	August 20, 2002
Moore et al.	US 2009/0092466 A1	April 9, 2009
Tai et al.	US 2012/0038014 A1	February 16, 2012

REJECTIONS

1. Claims 1, 4, 5, 16, 18–21, 23, 24, 26[2]–30, and 32 are rejected under 35 U.S.C. § 103 as unpatentable over Yamamoto in view of Mirkarimi, Miyanaga, and Moore.

2. Claims 6, 17, and 31 are rejected under 35 U.S.C. § 103 as unpatentable over Yamamoto in view of Mirkarimi, Miyanaga, and Moore, and further in view of Tai.

DISCUSSION

Appellant does not offer separate arguments for any claims (*see*, Appeal Br. 15, 16). Accordingly, we select claim 1 as representative and focus our discussion on its rejection over the combination of Yamamoto, Mirkarimi, Miyanaga, and Moore.

Summary of the rejection. The Examiner finds that Yamamoto discloses a method of forming a wiring structure with multiple layers of

[2] The statement of the rejection states that claims "36–30" are part of this rejection (Final Act. 3). However, based on the details of the rejection (*see*, Final Act. 11) it is apparent that this is a typographical error and that it should read "26–30."

wires which, according to the Examiner, corresponds to the claimed film stack on a substrate (Final Act. 3, citing Yamamoto, Title,14:35–40). The Examiner further finds that Yamamoto discloses depositing an oxide layer using a tetraethylorthosilicate (TEOS) precursor, depositing an adhesion layer comprising tungsten nitride onto the oxide layer, and depositing a metal layer comprising tungsten on the adhesion layer (Final Act. 3–4, citing Yamamoto 12:35–45, 13:49–67, 15:30–55, 19:1–30, 28:60–67, and 29:1–5). The Examiner also finds that the adhesion layer and the metal layer have a second thickness of 350–1700Å, and that the sequential deposition of an oxide layer, an adhesion layer, and a metal layer can be repeated (Final Act. 4).

The Examiner finds that Yamamoto does not teach (1) that the metal layer and the adhesion layer form a stress neutral structure, and (2) that the metal layer and the adhesion layer have a combined thickness of less than 200Å (Final Act. 4).

With regards to difference (1), the Examiner further finds that Mirkarimi is directed towards adjusting multilayer film stress induced deformation and teaches stacks that are stress neutral result in little to no deformation of the underlying substrate (Final Act. 4, citing Mirkarimi, Abstract). The Examiner determines that it would have been obvious to incorporate Mirkarimi's teachings of stress neutral stacks into Yamamoto's process because doing so would "predictably reduce[] deformation of the substrate and would have predictably improved the wiring structure of [Yamamoto] by reducing" its wiring structure (Final Act. 4).

With regards to difference (2), the Examiner finds that Miyanaga teaches that its nitride layer can have a thickness of 0.01 nm (i.e., 0.1Å)

(Miyanaga 6:30–45). Because the Examiner finds that Yamamoto teaches that its metal layer has a thickness of 50–200Å, the Examiner determines that combining the Miyanaga's nitride layer with Yamamoto's metal layer would yield a combined thickness of 50.1–200.1Å, which overlaps with the claimed range of less than or equal to 200Å (Final Act. 5).

Finally, the Examiner relies on Moore as suggesting the use of a plurality of processing chambers in a multichamber processing system and determines that it would have been obvious to apply this to Yamamoto's method to increase manufacturing throughput (Final Act. 5–6).

Appellant's arguments. Appellant argues, inter alia,[3] that the evidence of record does not support the Examiner's finding that Yamamoto teaches a "depositing an oxide layer using tetraethylorthosilicate (TEOS), the oxide layer having a first thickness of less than or equal to 250 Å" (Appeal Br. 8–9). The Examiner finds that this Yamamoto's layer 12 corresponds to the claimed oxide layer (Final Act. 13[4]). With regards to the thickness requirement, the Examiner finds that this limitation is taught by Yamamoto at column 19: "[Yamamoto] further teaches that the underlying layer [12] can be less than or equal to 250Å (col. 19, lines 1-30)" (*id.*; *see also*, Final Act. 3, and Ans. 3).

However, the evidence of record does not support the Examiner's finding that Yamamoto teaches that its layer 12 meets the claimed thickness

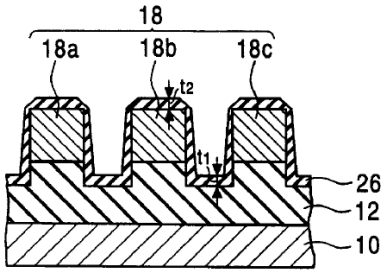
[3] Because we determine the two arguments discussed herein persuade us of reversible error, we do not address the remaining arguments.
[4] The Examiner writes: "it is apparent that [Yamamoto] discloses a[n] underlying layer (12) with a thickness of less than or equal to 250Å" (Final Act. 13).

requirement. The passage cited by the Examiner to support this finding reads as follows:

> In conventional wiring structures, a film of silicon oxide, silicon oxynitride, silicon nitride or the like is used as the underlying film. In contrast, according to this embodiment, a fluorinated silicon oxide film is used as the underlying film **26** for the low dielectric constant film **28**. As a result, the wiring capacitance can be further effectively reduced. It was not obvious that a fluorinated silicon oxide film could be used as an underlying film. . . . As a result, by using a fluorinated silicon oxide film rather than a silicon oxide film the thickness of the underlying film can be reduce [sic]. For example, t**l** can be thinned to less than 25 nm, and can be thinned to around 10 nm, depending on various conditions. Accordingly, it is possible to use this method even when the space between the wires is further decreased due to the progress of miniaturization.

(Yamamoto, 19:1–35, emphasis added). As shown in the passage above, it is apparent that the layer which has a thickness of less than 25 nm (250Å) is "underlying film **26**" as shown, for example, in Yamamoto's FIG. 5B reproduced below:

FIG. 5B



Yamamoto's FIG. 5B shows a step in Yamamoto's process to create a wiring structure.

As can be seen from the Figure above, the thickness t_1 referenced as being less than 25 nm is not the thickness of layer 12, which, as noted above,

the Examiner finds corresponds to the claimed oxide layer. Thickness t**1** instead is the thickness of layer 26, which is what is described by Yamamoto in the passage from column 19 quoted above.

Accordingly, the Examiner's finding that Yamamoto discloses "depositing an oxide layer using tetraethylorthosilicate (TEOS), the oxide layer having a first thickness of less than or equal to 250 Å" is not supported by the evidence.

The Examiner has the initial burden of establishing a prima facie case of obviousness based on an inherent or explicit disclosure of the claimed subject matter under 35 U.S.C. § 103. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992) ("[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability."). To establish a prima facie case of obviousness, the Examiner must show that each and every limitation of the claim is described or suggested by the prior art or would have been obvious based on the knowledge of those of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988).

In this instance, the Examiner has not adequately shown that the thickness limitation discussed above would have been obvious in view of the cited art.

Additionally, Appellant argues that a person of skill in the art would not have had a reason to combine Yamamoto and Miyanaga as set forth in the rejection (Appeal Br. 11–13). The Examiner finds that Miyanagi discloses multilayer wiring structures for integrated circuits, and also discloses a nitride layer having a thickness of 0.01 nm (i.e. 0.1Å) used in a metal wire stack (Final Act. 4–5). The Examiner determines that it would

have been obvious to use Miyanagi's 0.01 nm thick nitride layer in Yamamoto's process in place of the described 30–150 nm thick nitride layer because "it is recognized in the art of wiring structures for integrated circuits to use a thickness of 0.1 Å for the nitride layer in the metal wiring stack and thus the use of such a thickness would have predictably been suitable as the thickness for the nitride layer of [Yamamoto]" (Final Act. 5). This combination would, according to the Examiner yield a combined thickness of the metal layer and the nitride layer in Yamamoto which overlaps with the claimed thickness of under 200 Å.

However, the nitride layer in Yamamoto serves to prevent copper diffusion (Yamamoto, 28:62–63), and is at least 3000 times thicker than the nitride layer in Miyanaga (30 nm v. 0.01 nm). The Examiner has not provided a sufficient supported rationale that a person of skill in art would have understood that a 0.01 nm thick nitride layer could be substituted for a 30 nm nitride layer designed to prevent copper diffusion.

Accordingly, Appellant has demonstrated reversible error in the Examiner's explanation of why a person of skill in the art would have combined the teachings of Miyanaga and Yamamoto as set forth in the rejection. This is a second reason to reverse the rejection.

Therefore, we reverse the rejection of claim 1 and the claims dependent thereon. Because the other independent claims on appeal recite a similar limitations, we also reverse their rejection and the rejection of their dependent claims.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 4, 5, 16, 18–21, 23, 24, 26–30, 32	103	Yamamoto, Mirkarimi, Miyanaga, Moore		1, 4, 5, 16, 18–21, 23, 24, 26–30, 32
6, 17, 31	103	Yamamoto, Mirkarimi, Miyanaga, Moore, Tai		6, 17, 31
Overall Outcome				1, 4–6, 16–21, 23, 24, 26–32

REVERSED