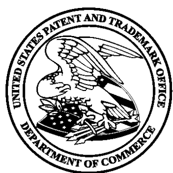

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HIROAKI NIIMI and SEUNG-CHUL SONG

Appeal 2019-006404
Application 14/325,787
Technology Center 2800

Before TERRY J. OWENS, JEFFREY T SMITH, and BRIAN D. RANGE, *Administrative Patent Judges.*

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), the Appellant[1] appeals from the Examiner's decision to reject claims 1–18. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). The Appellant identifies the real party in interest as Texas Instruments Incorporated. Appeal Br. 3.

CLAIMED SUBJECT MATTER

The claims are directed to REPLACEMENT METAL GATE PROCESS FOR CMOS INTEGRATED CIRCUITS. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method of forming an integrated circuit structure at a semiconducting surface of a body, the integrated circuit structure including first and second transistors of opposite channel conductivity types, comprising:
>
> forming first and second dummy gate electrodes overlying a dummy gate dielectric material on the semiconducting surface, the second dummy gate electrode overlying a region of a first conductivity type, and the first dummy gate electrode overlying a region of a second conductivity type, the second conductivity type opposite the first conductivity type;
>
> forming source/drain regions of the first conductivity type into the region of second conductivity type, at locations on opposite sides of the first dummy gate electrode;
>
> forming source/drain regions of the second conductivity type into the region of first conductivity type, at locations on opposite sides of the second dummy gate electrode;
>
> depositing filler dielectric between the first and second dummy gate electrodes;
>
> patterning a mask layer over the second dummy gate electrode, the mask layer exposing the first dummy gate electrode;
>
> removing the first dummy gate electrode and its underlying dummy gate dielectric material to define a gap between filler dielectric structures and to expose a portion of the region of second conductivity type;
>
> forming a first dielectric interface layer at the exposed portion of the region of second conductivity type;
>
> depositing a first high-*k* dielectric layer overall;
>
> then depositing a first metal gate layer, the first metal gate layer comprising a metal or metal compound;
>
> then depositing a first fill metal to fill the gap at the location from which the first dummy gate electrode was removed;

then performing a first chemical-mechanical polishing (CMP) to remove portions of the first fill metal and first metal gate layer and planarize the integrated circuit structure to expose a top surface of the second dummy gate electrode;

removing the second dummy gate electrode and its underlying dummy gate dielectric material to define a gap between filler dielectric structures and to expose a portion of the region of first conductivity type;

forming a second dielectric interface layer at the exposed portion of the region of first conductivity type;

depositing a second high-*k* dielectric layer overall;

then depositing a second metal gate layer, the second metal gate layer comprising a metal or metal compound;

then depositing a second fill metal to fill the gap at the location from which the second dummy gate electrode was removed; and

then performing a second CMP to planarize the integrated circuit structure and to expose top surfaces of the first and second fill metal and of the filler dielectric;

wherein the first metal gate layer and the second metal gate layer differ from one another in composition with the second metal gate layer being removed from over the first transistor and the first metal gate layer being removed from over the second transistor.

The prior art relied upon by the Examiner is:

Name	Reference	Date
Doczy	US 2006/0017098 A1	Jan. 26, 2006
Waite	US 2009/0087974 A1	Apr. 2, 2009
Lee ’818	US 2010/0124818 A1	May 20, 2010
Chuang	US 2012/0001259 A1	Jan. 5, 2012
Kwon	US 2012/0132998 A1	May 31, 2012
Lee ’758	US 2012/0261758 A1	Oct. 18, 2012
Liu	US 2013/0082332 A1	Apr. 4, 2013

REJECTIONS

Claims 1–18 stand rejected under 35 U.S.C. § 103(a) as follows: claims 1, 2, 8, and 10–12 over Waite in view of Doczy; claims 10 and 18 over Waite in view of Doczy and Liu; claims 3–7 and 13–16 over Waite in view of Doczy, Lee ’758, Kwon, and Chuang; and claims 9 and 17 over Waite in view of Doczy and Lee ’818.

OPINION

We need to address only claim 1.[2] That claim requires 1) forming a first dielectric interface layer (32p) at the exposed portion of an integrated circuit’s region (24n) of second conductivity type; depositing a first high-k dielectric layer (34p) overall; then depositing a first metal gate layer (35p); then depositing a first fill metal (38p) to fill the gap at the location from which a first dummy gate electrode (40-right side) was removed, and 2) forming a second dielectric interface layer (32n) at the exposed portion of an integrated circuit’s region (24p) of first conductivity type; depositing a second high-k dielectric layer (34n) overall; then depositing a second metal gate layer (35n); then depositing a second fill metal (38n) to fill the gap at the location from which a second dummy gate electrode (40-left side) was removed.

Waite 1) forms a dielectric interface layer (112A) at the exposed portion of an integrated circuit region (117-left side; Fig. 1i); deposits a first high-k dielectric layer (124) overall (Fig. 1j); then deposits a first metal-containing material (125) to fill the gap at the location from which a first dummy gate electrode (110-left side; Fig. 1a) was removed (Figs. 1j, 1k),

[2] Claim 11, which is the only other independent claim, has limitations similar to those in claim 1.

2) forms a dielectric interface layer (112A) at the exposed portion of another integrated circuit region (117-right side; Fig. 1n); deposits a second high-k dielectric layer (128) overall (Fig. 1o); then deposits a second metal-containing material (129) to fill the gap at the location from which a second dummy gate electrode (110-right side; Fig. 1a) was removed (Figs. 1o, 1p), 3) forms a recess (110R) in each gap-filling material (125, 129; Fig. 1q), and 4) fills those recesses with a conductive material (131; Figs. 1r, 1s).

Doczy 1) forms a dielectric interface layer (105) at the exposed portion of an integrated circuit region (101) (Fig. 1a); removes that dielectric layer and then deposits a first high-k dielectric layer (115) overall (Figs. 1b, 1c); then deposits a first metal gate layer (116) (Fig. 1d); then deposits a first metal (121) to fill the gap at the location from which a first dummy gate electrode (104) was removed (Figs. 1e, 1f), and 2) forms a second dielectric interface layer (107) at the exposed portion of another integrated circuit region (102) (Fig. 1a); removes that dielectric layer and then deposits a second high-k dielectric layer (117) overall (Figs. 1g, 1h); then deposits a second metal gate layer (120) (Fig. 1h); then deposits a second fill metal (118) to fill the gap at the location from which a second dummy gate electrode (106) was removed (Figs. 1h, 1i).

The Examiner finds that

> modifying the metal fill process of Waite et al. with the metal fill process of Doczy et al. would actually result in the following sequence: (1) deposit metal 125 (Waite et al., Fig. 1j, though it would look like the deposit of metal 116 as illustrated in Doczy et al., Fig. 1d); (2) deposit metal 131 (Waite et al., Fig. 1r, though it would look like the deposit of metal 121 as illustrated in Doczy et al., Fig. 1e); (3) first CMP (Waite et al., Fig. 1k, though the gate structure at this point would look like Doczy et al., Fig. 1f); (4) deposit metal 129 (Waite et al., Fig. 1o, though it would look like the deposit of metal 120 as

> illustrated in Doczy et al., Fig. 1h); (2) deposit metal 131 (Waite et al., Fig. 1r, though it would look like the deposit of metal 118 as illustrated in Doczy et al., Fig. 1h); (3) second CMP (Waite et al., Fig. 1p, though the gate structure at this point would look like Doczy et al., Fig. 1i). As can be readily observed, Waite et al., when modified as taught by Doczy et al. and proposed by Examiner, would result in TWO CMP steps, instead of THREE CMP steps in Waite et al.'s disclosed process (Waite et al. Figs. 1k, 1p, and 1s).

Ans. 4.

Setting forth a prima facie case of obviousness requires establishing that the applied prior art would have provided one of ordinary skill in the art with an apparent reason to modify the prior art to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

As indicated above, the Examiner finds that the Appellant's claimed method would result if Waite's metal-containing conductive material 125 (Figs. 1j, 1k) lined the trench like Doczy's metal layer 116 (Fig. 1f) instead of filling it, and Waite's conductive material 131 filled the trench instead of subsequently filling recesses 110R (Figs. 1q, 1r). The Examiner, however, does not establish that the applied references would have provided one of ordinary skill in the art with an apparent reason to make those modifications. Thus, the record indicates that the Examiner used impermissible hindsight in rejecting the Appellant's claims. *See In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967) ("A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art."). Accordingly, we reverse the rejections.

CONCLUSION

The Examiner's rejections are reversed.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 2, 8, 10–12	103(a)	Waite, Doczy		1, 2, 8, 10–12
10, 18	103(a)	Waite, Doczy, Liu		10, 18
3–7, 13–16	103(a)	Waite, Doczy, Lee ’758, Kwon, Chuang		3–7, 13–16
9, 17	103(a)	Waite, Doczy, Lee ’818		9, 17
Overall Outcome				1–18

REVERSED