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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/355,498 | 11/18/2016 | Michael Simcoe | 1012-1625 / 2016P51324 US | 9787 |

57579 7590 09/14/2020

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|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2843 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 09/14/2020 | ELECTRONIC |

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* MICHAEL SIMCOE

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Appeal 2019-005923
Application 15/355,498
Technology Center 2800

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Before JEFFREY B. ROBERTSON, MICHAEL G. McMANUS, and MERRELL C. CASHION, JR., *Administrative Patent Judges*.

McMANUS, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] seeks review of the Examiner's decision to reject claims 1–19. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Infineon Technologies AG. Appeal Brief dated March 18, 2019 ("Appeal Br.") 2.

## CLAIMED SUBJECT MATTER

The present application generally relates to RF power packages having tuning lines. Specification filed Nov. 18, 2018 ("Spec.") ¶ 1. It is conventionally known that impedance matching is needed in RF power packages. *Id.* ¶ 2. The Specification teaches that wire bonds are conventionally used for impedance matching, however, wire bonds are complex and expensive to implement. *Id.* The Specification further teaches that there is a need for an alternative impedance matching/transformation solution for RF power packages. *Id.*

To that end, the Specification teaches an RF power package having a plurality of planar tuning lines electrically connecting the die output terminal to the package output terminal. *Id.* ¶ 3. Such tuning lines are shaped so as to transform the output impedance at the die output terminal to a higher target level. *Id.* Figure 1 of the Drawings is reproduced below.

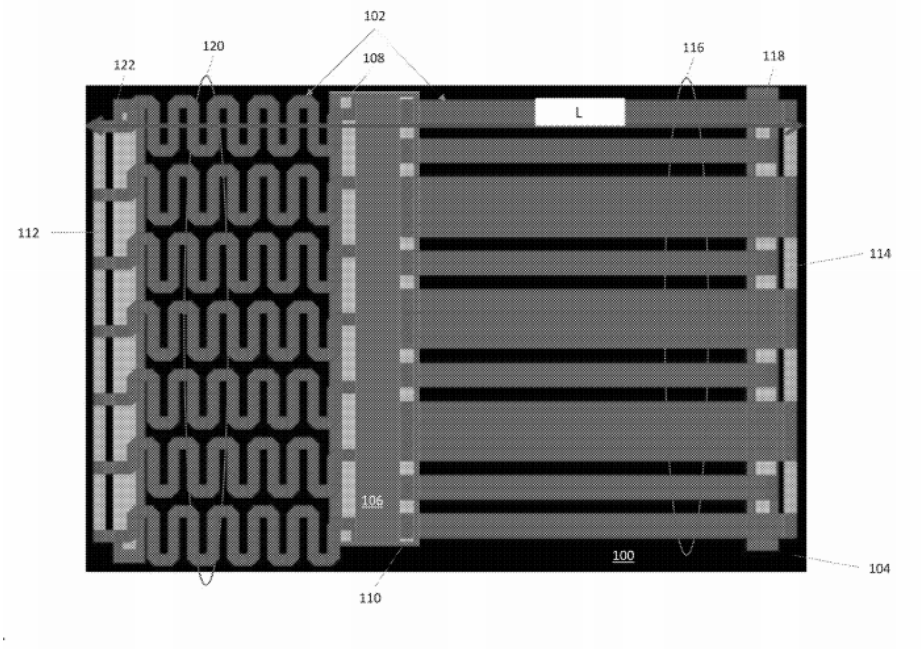

Figure 1 "illustrates a top-down plan view an embodiment of an RF power package." *Id.* ¶ 17. It depicts die 106 attached to substrate 100. *Id.* It further shows die output terminal 110 and package output terminal 114 connected by planar tuning lines 116.

Claim 1 is illustrative of the subject matter on appeal and is reproduced below with certain limitations bolded for emphasis:

> 1. An RF power package, comprising:
>
> a substrate having a metallized part and an insulating part;
>
> **an RF power transistor die embedded in or attached to the substrate**, the RF power transistor die having a die input terminal, a die output terminal, an input impedance and an output impedance;
>
> a package input terminal formed in the metallized part or attached to the insulating part of the substrate;
>
> a package output terminal formed in the metallized part or attached to the insulating part of the substrate; and
>
> a first plurality of planar tuning lines formed in the metallized part of the substrate and electrically connecting the die output terminal to the package output terminal,
>
> wherein the first plurality of planar tuning lines is shaped so as to transform the output impedance at the die output terminal to a higher target level at the package output terminal.

Appeal Br. 15 (Claims App.) (reformatted for clarity)

## REFERENCES

The Examiner relies upon the following prior art:

| Name | Reference | Date |
|---|---|---|
| Ikeda et al. ("Ikeda") | US 5,270,668 | Dec. 14, 1993 |
| Salmela et al. ("Salmela") | US 6,639,487 B1 | Oct. 28, 2003 |
| Abdo et al. ("Abdo") | US 2017/0085228 Al | Mar. 23, 2017 |

## REJECTIONS

The Examiner maintains the following rejections:

1. Claims 1–8, 10–15, and 17–19 are rejected under 35 U.S.C. § 103 as being unpatentable over Abdo in view of Salmela. Final Action dated Oct. 19, 2018 ("Final Act.") 2–10.
2. Claims 7, 9, 14, and 16 are rejected under 35 U.S.C. § 103 as being unpatentable over Abdo in view of Salmela and Ikeda. *Id.* at 10–13.

## DISCUSSION

**Rejection 1.** The Examiner rejects claims 1–8, 10–15, and 17–19 as obvious over Abdo in view of Salmela. *Id.* at 2–10. In support of the rejection, the Examiner finds that Abdo teaches "an RF power package, comprising: a substrate having a metallized part and an insulating part (die 450, comprising a plurality of dielectric and conductive layers, para [0046])." *Id.* at 2. The Examiner further finds that Abdo teaches "an RF power transistor (transistor 420, noted as being high-power RF amplifier devices in para [0001]) die embedded in or attached to the substrate." *Id.* Figure 6 of Abdo is reproduced below.

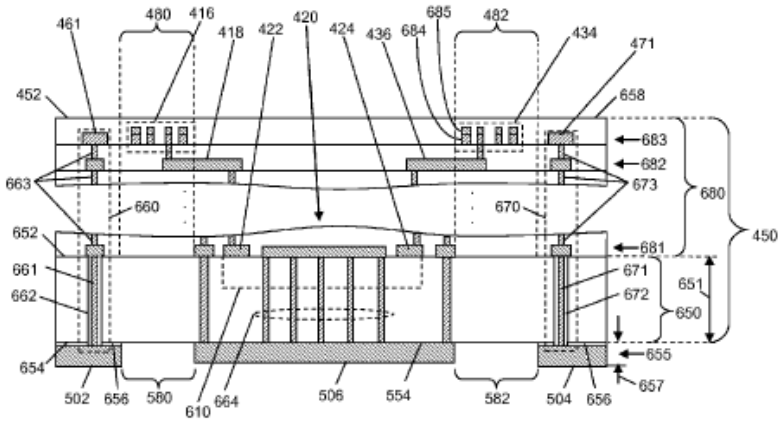


Figure 6 is a cross-sectional side view of the semiconductor die 450 of Abdo. Abdo ¶ 11. Figure 6 depicts substrate 650 and a plurality of dielectric and conductive layers 680 (referred to as "build-up layers") as well as transistor 420. *Id.* ¶¶ 46, 48.

Appellant alleges error on several bases. Appeal Br. 4–9. First, Appellant argues that the Examiner errs in equating "element 450 in the Abdo reference to Appellant's claimed substrate and element 420 to Appellant's RF power transistor die." *Id.* at 5; *see also id.* at 4–7. Appellant contends that structure 450 of Abdo is a semiconductor die that includes substrate 650 and a plurality of dielectric and conductive layers 680 formed over the substrate. *Id.* at 6. Appellant further asserts that element 420 is not a die but is merely a transistor formed in Abdo's semiconductor die 450. *Id.* at 7.

In the Answer, the Examiner determines that claims 1 and 11 do not require the die and the substrate to be separate and distinct components. Examiner's Answer dated June 10, 2019 ("Ans.") 18. The Examiner directs us to claim 1's requirement that the package include "an RF power transistor die *embedded in* or attached to the substrate." *Id.* (emphasis added). The

Examiner determines that the broadest reasonable interpretation of "embedded" is "to be or become fixed or incorporated, as into a surrounding mass." *Id.* As a consequence, the Examiner asserts, claims 1 and 11 do not require an embedded RF power transistor die in a substrate to have separate and distinct physical boundaries from the substrate. *Id.*

The Examiner further determines that element 420 of Abdo "includes an active area 610 . . . in the semiconductor substrate 650 that includes portions of the circuit of the transistor . . . . As such, transistor 420 and its corresponding active area 610 may be identified as an RF power transistor die." *Id.* at 19.

Thus, the rejection is based on the Examiner's findings that the substrate portion of the die taught by Abdo (structure 650 in Figure 6) teaches the "substrate" limitation and the transistor of Abdo (structure 420 in Figure 6) teaches the "RF power transistor die embedded in or attached to the substrate."

In evaluating Appellant's arguments, we consider the meaning of the term "die."

The Specification does not provide any special definition of the term "die." The Drawings depict die 106 as a structure attached to substrate 100. *See* Figs. 1, 2. Appellant offers several exhibits bearing upon the meaning of the term "die." One provides as follows:

> Electronic circuit of the semiconductor device is arranged on a semiconductor wafer. After performing various processes such as exposure and etching of the circuit patterns, die is the minimum unit of the semiconductor device to be cut out individually. Built-in to the package, by wiring the pins of the semiconductor of the contact and the IC package, IC chip is completed.

Appeal Br., Ex. D (Hitachi Semiconductor Glossary[2]). The other exhibits are generally similar. Thus, we conclude that a die, considered alone, is a portion (unit) of semiconducting material to which circuit patterns are added and which is subsequently cut out (singulated) from a larger wafer.

The Examiner finds that transistor 420 is a die. We are persuaded that this finding is erroneous. Abdo plainly teaches that structure 450 shown in Figures 4 and 6 is a die. Abdo ¶ 46. This is consistent with the plain meaning of the term "die." Transistor 420 is a component of the die but is not, itself, a die. *See* Abdo, Fig. 4.

Second, Appellant argues that the prima facie case of obviousness is flawed because a person of ordinary skill in the art would not have had reason to combine the teachings of Abdo and Salmela. Appeal Br. 7–9. In the Final Office Action, the Examiner determines that "it would have been obvious to one of ordinary skill in the art to use the uninterrupted planar tuning line of Salmela for the first plurality of impedance matching circuits of Abdo et al. as art-recognized alternative impedance matching able to provide the same function." Final Act. 3.

Appellant argues that Abdo concerns amplifier circuits while Salmela concerns microwave monolithic IC (MMIC) packages. *Id.* at 7–8. In this regard, the Examiner finds that "Abdo may be considered an MMIC package (being concerned with monolithic implementations, para [0034]) and has signal line feedthroughs (input and output circuits 110 & 130, both of which

[2] https://www.hitachi-hightech.com/global/products/device/semiconductor/words.html#Die, dated March 7, 2019.

may have impedance matching circuits." Ans. 21. This finding is unrebutted.

Appellant additionally contends that the Examiner "has failed to adequately explain exactly how one of ordinary skill in the art would modify Abdo's semiconductor die 450 to include the alleged planar tuning lines of the Salmela reference." *Id.* at 8–9. The Examiner need not explain the details of physical combination. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference," *In re Keller*, 642 F.2d 413, 425 (CCPA 1981), but rather whether "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention," *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007).

Accordingly, Appellant has not shown error on this basis.

Third, Appellant argues that Salmela teaches away from the claims. Appeal Br. 9–10. Appellant argues that "the Salmela reference explicitly states that integrating the coplanar coupling structures shown in Figures 1a, 1b and 2 of Salmela into a GaAs chip 'complicates the structure of the IC and causes faulty connections as well as damaged chips in the manufacturing process.'" *Id.* at 9 (citing Salmela 3:22–34). This is not persuasive of error. The Examiner finds that the cited teaching is limited to chips having metallized vias. Ans. 23. This finding in unrebutted.

We find Appellant's first argument (regarding the "die" and "substrate" limitations) to be persuasive. Accordingly, we determine that the Examiner erred in rejecting claims 1 and 11 as obvious over Abdo in view of Salmela.

*Claim 2*

Appellant argues that the rejection of claim 2 as obvious over Abdo in view of Salmela is erroneous. Appeal Br. 10. Claim 2 depends from claim 1 and further requires that "the substrate comprises a ceramic body and a patterned metallization applied to the ceramic body, and wherein the patterned metallization forms the metallized part of the substrate." *Id.* at 15 (Claims App.).

In the Final Office Action, the Examiner finds that Salmela teaches that ceramic substrates are a normal multilayer substrate technology that is known in the art. Final Act. 4. The Examiner finds that the build-up layers of Abdo's die 450 form a "metallized part of the substrate" (considering the die of Abdo to be the substrate of the claim). *Id.* The Examiner further determines that it would have been obvious to one of ordinary skill in the art to use ceramic for the dielectric layers of the substrate of Abdo. *Id.*

Appellant argues that "it would be illogical to modify Abdo's semiconductor die 450 so that the semiconductor substrate 650 is a ceramic body with an applied patterned metallization." *Id.* at 10. Appellant further asserts that "[i]f Abdo's substrate 650 were indeed a ceramic body with an applied patterned metallization . . . no active devices could be formed in the substrate 650." *Id.* (emphasis omitted).

In the Answer, the Examiner indicates that the proposed combination is not to replace the semiconductor substrate 650 with a ceramic body. Ans. 24. Rather, the Examiner states, the combination posits that the general dielectric layers of build-up layers 680 be made of ceramic as taught by Salmela.

The Reply Brief does not address claim 2.

Appellant's arguments appear to be predicated on the notion that the hypothetical combination includes substitution of a ceramic body for substrate 650. This is inconsistent with the rejection as clarified in the Answer. Accordingly, Appellant has not shown error in this regard. Despite this, because the Examiner relies on findings made in support of the rejection of claim 1, the rejection of claim 2 will not be sustained.

*Claims 3 and 4*

Appellant argues that the rejection of claims 3 and 4 as obvious over Abdo in view of Salmela is erroneous. Appeal Br. 10–12. Claim 3 depends from claim 1 and further requires that the "substrate is a printed circuit board." Appeal Br. 15 (Claims App.). Claim 4 depends from claim 1 and further requires that the RF power transistor die is embedded in a first insulating material of the substrate. Both rejections depend upon the finding that Abdo's die satisfies the "substrate" requirement (Final Act. 4–5). As a consequence, both rejections are erroneous.

*Claims 6, 8, 13, and 15*

Claims 6, 8, 13, and 15 depend from claim 1 or claim 11 and further require a capacitor. Claims 6 and 13 require that the capacitor is electrically connected between the die output terminal and the package output terminal. Appeal Br. 16, 19 (Claims App). Claims 8 and 15 require a capacitor electrically connected between the die input terminal and the package input terminal. *Id.* at 17, 19–20.

The Examiner relies on DC blocking capacitor 136 of Abdo as teaching a capacitor electrically connected between the die output terminal and the package output terminal (claims 6 and 13). Final Act. 5. The Examiner additionally finds that DC blocking capacitor 317 shown in Abdo's Figure 3 teaches electrically connected between the die input terminal and the package input terminal as required by claims 8 and 15. *Id.* at 6–7.

Appellant argues that Abdo's Figures 1 and 3 are merely circuit schematics which cannot be relied upon to teach structural detail. Appeal Br. 12–13. Appellant further argues that there is no inherent disclosure of a capacitor located as claimed.

In the Answer, the Examiner finds that Abdo's "Figs. 1-3 clearly show the capacitors . . . implemented on the semiconductor substrate (650) . . . . Furthermore, Fig. 8 (a view of Fig. 4) clearly shows capacitors 414 & 432 as being embedded in the substrate (build up layers 680)." Ans. 26.

As above, resolution of the present argument turns on whether one accepts the Examiner's view of the terms "die" and "substrate" being taught by Abdo. As we do not accept the Examiner's findings, we determine that the structures identified by the Examiner are within the die and not electrically connected between the die terminal and the package terminal. Accordingly, Appellant has shown error in this regard.

*Claims 10 and 17*

Claims 10 and 17 depend from claims 1 and 11, respectively, and further require an "additional RF power transistor die" embedded in or attached to the substrate. Appeal Br. 17–18, 20.

The Examiner finds that this is satisfied by the multiple transistor circuits (420, 421) taught within the die of Abdo. Final Act. 7–8.

As we have not accepted the Examiner's findings regarding Abdo's teaching of a die and substrate, we do not accept the Examiner's finding that the several transistors taught by Abdo satisfy the claims' requirement of additional dies within the package.

**Rejection 2.** The Examiner rejects claims 7, 9, 14, and 16 as obvious over Abdo in view of Salmela and Ikeda. Final Act. 10–13. Claims 7 and 9 depend from claim 1. Appeal Br. 16, 17 (Claims App.). Claims 14 and 16 depend from claim 11. *Id.* at 19, 20. The Examiner relies on the same findings made in rejecting claims 1 and 11 in support of the rejection of claims 7, 9, 14, and 16. Final Act. 11 ("as applied to claims 1 & 11 above"). The rejections of claims 1 and 11 have been found to be erroneous. Accordingly, we do not sustain the rejection of claims 7, 9, 14, and 16.

## CONCLUSION

The Examiner's rejections are reversed.

In summary:

| Claims Rejected | 35 U.S.C. § | Reference(s)/Basis | Affirmed | Reversed |
|---|---|---|---|---|
| 1–8, 10–15, 17–19 | 103 | Abdo, Salmela | | 1–8, 10–15, 17–19 |
| 7, 9, 14, 16 | 103 | Abdo, Salmela, Ikeda | | 7, 9, 14, 16 |
| **Overall Outcome** | | | | 1–19 |

REVERSED