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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JARED ZERBE, PAK SHING CHAU, and
WILLIAM\ FRANKLIN STONECYPHER

Appeal 2019-005861
Application 15/143,299[1]
Technology Center 2100

Before MAHSHID D. SAADAT, MARC S. HOFF, and
IRVIN E. BRANCH, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of claims 2–6, 8–16, and 18–21.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellant's invention is a method and apparatus for evaluating and optimizing a signaling system. A pattern of test information is generated in a transmit circuit, produced by a linear feedback shift register (LFSR). Spec.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant states the real party in interest is Rambus Inc. Appeal Br. 1.

[2] Claim 1 has been cancelled. Claims 7 and 17 do not stand rejected.

6. A similar pattern of information is generated in a receive circuit and is used as a reference. *Id.* The transmit circuit can operate in a normal mode or a test mode. In the normal mode, a shift register receives data via a data input, and shifts the bits of data to the right, providing each bit as an output. Spec. 9. In the test mode, the shift register and a test loop function to generate a test pattern for transmission. *Id.*

Claim 2 is exemplary of the claims on appeal:

> 2. An integrated circuit to communicate with a receive circuit via a conductive medium which is external to the integrated circuit, the integrated circuit comprising:
>
> a connection to electrically connect to the conductive medium;
>
> an output driver to transmit a serial output signal via the connection; and
>
> a shift register to receive a data word and to serially output bits of data to the output driver dependent on the data word, the output driver to transmit the serial output signal dependent on the bits of data;
>
> wherein the shift register is part of a linear feedback shift register circuit of the integrated circuit, the shift register is operable in a first mode, in which the data word is serially output by the shift register to form the bits of data, and
>
> the shift register is operable in a second mode, in which the linear feedback shift register circuit deterministically generates the bits of data in dependence on combining the data word with feedback bits generated by the linear feedback shift register circuit.

The Examiner relies upon the following prior art in rejecting the claims on appeal:

NAME	REFERENCE	DATE
Thomas et al. "Thomas"	US 4,586,159	Apr. 29, 1986
Lee et al. "Lee"	US 5,029,171	July 2, 1991
Bhawmik	US 5,680,543	Oct. 21, 1997

Claims 2–6, 8, 10,[3] 11, 13–16, 18, 20, and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lee.

Claims 9 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Bhawmik.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Thomas.

Throughout this decision, we make reference to the Appeal Brief ("Appeal Br.," filed Feb. 28, 2019), the Reply Brief ("Reply Br.," filed July 31, 2019), and the Examiner's Answer ("Ans.," mailed June 30, 2019) for their respective details.

ISSUES

Appellant's arguments present us with the following issues:

1. Does Lee teach the claimed integrated circuit?

2. Does Lee teach a shift register that is part of a linear feedback shift register circuit?

3. Does Lee teach a shift register operable in a first mode, in which a data word is serially output by the shift register to form bits of data, and

[3] Claim 10 is not included in the Examiner's statement of rejection, but is discussed in the body of the rejection. Final Act. 16.

operable in a second mode in which a linear feedback shift register circuit deterministically generates the bits of data in dependence on combining the data word with feedback bits generated by the linear feedback shift register circuit?

PRINCIPLES OF LAW

"A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference." *See In re Buszard,* 504 F.3d 1364, 1366 (Fed. Cir. 2007) (quoting *In re Paulsen*, 30 F.3d 1475, 1478–79 (Fed. Cir. 1994)). Anticipation of a claim requires a finding that the claim at issue reads on a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (quoting *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 781 (Fed. Cir. 1985)).

ANALYSIS

Claims 2–6, 8, 10, 11, 13–16, 18, 20, and 21

Independent claims 2 and 13 recite "[a]n integrated circuit to communicate with a receive circuit via a conductive medium [conductive media] which is [are] external to the integrated circuit." Independent claims 2 and 13 further recite a shift register which "is part of a linear feedback shift register circuit." Independent claims 2 and 13 further recite that the shift register "is operable in a first mode, in which the data word is serially output by the shift register to form the bits of data," and "is operable in a second mode, in which the linear feedback shift register circuit deterministically generates the bits of data in dependence on combining the

data word with feedback bits generated by the linear feedback shift register circuit."

Appellant argues that Lee does not teach an integrated circuit. Appeal Br. 5. An "integrated circuit" is defined as "[a] complete circuit, including active and passive electronic devices and their interconnections, that is made on a single substrate." A "monolithic integrated circuit" has all the circuit components made into or on top of a single chip of semiconductor." Oxford Dictionary of Electronics and Electrical Engineering (5th Edition), 2018. https://www.oxfordreference.com/view/10.1093/acref/9780198725725.001.0001/acref-9780198725725-e-2377?rskey=AaYpKa&result=2384. Retrieved August 10, 2020. We agree with Appellant that Lee teaches several discrete electronic components, rather than a complete circuit made on a single substrate or on top of a single semiconductor chip. Thus, we find that Lee does not teach an "integrated circuit" as required by the claims.

The Examiner finds that Lee's four bit shift registers 156, 158 correspond to the claimed shift register. Final Act. 12. Lee teaches that shift registers 156 and 158 are part of Application Interface Unit 20, portrayed at the bottom right of Figure 1 and illustrated in detail in Figure 5. Appellant's claims also recite that the claimed shift register is part of a linear feedback shift register circuit. The Examiner finds that Lee's LFSR 16 and shift registers 156 and 158 are connected together to form a serial scan register chain. Final Act. 13; Lee, col. 8:36–38. Lee, however, discloses here only that shift registers 156 and 158 form such a serial scan register chain. Lee

does not teach that shift registers 156, 158 are part of a linear feedback shift register circuit, as the claims require.

Appellant further argues that Lee does not teach a shift register operable in a first mode in which a data word is serially output by the shift register to form bits of data, and operable in a second mode in which the LFSR deterministically generates the bits of data in dependence on combining the data word (received by the shift register) with feedback bits generated by the LFSR, as required in claim 2. Appeal Br. 7-9.

We agree with Appellant's contention that Lee does not teach structure in which a data word is processed in two different ways according to the mode of the shift register. Appeal Br. 8. We further find that the linear feedback shift register 16 of Lee, identified by the Examiner as corresponding to the LFSR of the claim, does not operate to deterministically generate the bits of data in dependence on combining the data word with feedback bits generated by the LFSR. We agree with Appellant that Lee teaches a structure where Application Interface Unit 20 effectively has a multiplexer that either selects an output of Lee's LFSR 16, or selects a signal from combinatorial logic system 164. Appeal Br. 7.

As a consequence of the deficiencies we find in Lee, we find that Lee does not teach all the limitations of independent claims 2 and 13. We do not sustain the § 102(b) rejection of claims 2–6, 8, 10, 11, 13–16, 18, 20, and 21 as being anticipated by Lee.

Claims 9 and 19

Claim 9 depends from independent claim 2, and claim 19 depends from independent claim 13.

We do not sustain the rejection of claims 2 and 13, *supra*. We have reviewed Bhawmik, and we find that Bhawmik does not remedy the deficiencies of Lee, described *supra*. Accordingly, we do not sustain the § 103(a) rejection of claims 9 and 19 over Lee and Bhawmik, for the reasons expressed *supra* with respect to the rejection over Lee alone.

Claim 12

Claim 12 depends from independent claim 2.

We do not sustain the rejection of claims 2 and 13, *supra*. We have reviewed Thomas, and we find that Thomas does not remedy the deficiencies of Lee, described *supra*. Accordingly, we do not sustain the § 103(a) rejection of claim 12 over Lee and Thomas, for the reasons expressed *supra* with respect to the rejection over Lee alone.

CONCLUSION

1. Lee does not teach the claimed integrated circuit.

2. Lee does not teach a shift register that is part of a linear feedback shift register circuit.

3. Lee does not teach a shift register operable in a first mode, in which a data word is serially output by the shift register to form bits of data, and operable in a second mode in which a linear feedback shift register circuit deterministically generates the bits of data in dependence on combining the data word with feedback bits generated by the linear feedback shift register circuit.

The Examiner's decision to reject claims 2–6, 8–16, and 18–21 is reversed.

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
2–6, 8, 10, 11, 13–16, 18, 20, 21	102	Lee		2–6, 8, 10, 11, 13–16, 18, 20, 21
9, 19	103	Lee, Bhawmik		9, 19
12	103	Lee, Thomas		12
Overall Outcome				**2–6, 8–16, 18–21**

REVERSED