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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes application details for John Tagle and examiner information for Benjamin T. Liu.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* JOHN TAGLE, DMITRY ZHILINSKY, and MICHAEL LILAND

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Appeal 2019-005541  
Application 14/198,923  
Technology Center 2800

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Before ROMULO H. DELMENDO, LINDA M. GAUDETTE, and  
LILAN REN, *Administrative Patent Judges*.

GAUDETTE, *Administrative Patent Judge*.

DECISION ON APPEAL<sup>1</sup>

The Appellant<sup>2</sup> appeals under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1–5, 7–12, and 14–17.<sup>3</sup>

We AFFIRM.

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<sup>1</sup> This Decision includes citations to the following documents: Specification filed March 6, 2014 (“Spec.”); Final Office Action dated August 3, 2018 (“Final Act.”); Appeal Brief filed January 4, 2019 (“Appeal Br.”); and Examiner’s Answer dated April 12, 2019 (“Ans.”).

<sup>2</sup> We use the word “Appellant” to refer to “applicant” as defined in 37 C.F.R. § 1.42. The Appellant identifies the real party in interest as Sensor Unlimited Inc. Appeal Br. 1.

<sup>3</sup> We have jurisdiction under 35 U.S.C. § 6(b).

### CLAIMED SUBJECT MATTER

The invention relates “to packaging for a focal plane array device including a photodiode array and a read out integrated circuit.” Spec. ¶ 2. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

1. An image sensor, comprising:
  - a package substrate comprising a recess and a raised pedestal of the package substrate within the recess extending from a base of the recess;
  - a read out integrated circuit (ROIC) physically attached to the raised pedestal;
  - a photodiode array (PDA) physically attached to the ROIC and electrically coupled therewith;
  - a printed circuit board (PCB) within the recess in the package substrate, wherein the PCB has an opening therein and the raised pedestal at least partially extends through the opening in the PCB; and
  - a plurality of bond wires that electrically couple the PCB to the ROIC, wherein the PDA is flip chip mounted to the ROIC and the plurality of bond wires are electrically coupled to the PDA through the ROIC.

Appeal Br. 10 (Claims App.). Claim 8, the only other appealed, independent claim, recites a method of forming an image sensor. *Id.* at 11.

### REJECTIONS

1. Claims 1, 2, 7–9, 14, and 15 are rejected under 35 U.S.C. § 103 as unpatentable over Tokiwa (JP 2007-049369 (A), published February 22, 2007, English translation) in view of Kalliopuska (US 2014/0284752 A1, published September 25, 2014).

2. Claims 3 and 10 are rejected under 35 U.S.C. § 103 as unpatentable over Tokiwa in view of Kalliopuska and Lee (US 5,379,187, issued Jan. 3, 1995).

3. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. § 103 as unpatentable over Tokiwa in view of Kalliopuska and Kinsman (US 2013/0221470 A1, published Aug. 29, 2013).

4. Claim 16 is rejected under 35 U.S.C. § 103 as unpatentable over Tokiwa in view of Kalliopuska and Tseng (US 2005/0099532 A1, published May 12, 2005).

5. Claim 17 is rejected under 35 U.S.C. § 103 as unpatentable over Tokiwa in view of Kalliopuska and Shiu (US 2005/0156301 A1, published July 21, 2005).

#### OPINION

As to independent claims 1 and 8, the Examiner found that Tokiwa discloses an image sensor and a method of forming an image sensor as claimed except for “a plurality of bond wires that electrically couple the PCB to the ROIC, wherein the PDA is flip chip mounted to the ROIC and the plurality of bond wires are electrically coupled to the PDA through the ROIC.” Final Act. 2, 4. The Examiner determined that the ordinary artisan would have formed Tokiwa’s image sensor with Kalliopuska’s flip chip mount “to keep short the signal paths between the sensor volume and the read-out element,” and would have replaced Tokiwa’s terminals with Kalliopuska’s wirebond “to provide an electrical connection that is both cost-effective and flexible.” *Id.* at 3, 5.

The Appellant argues that the Examiner reversibly erred in finding that the ordinary artisan would have had a reason to combine Tokiwa and

Kalliopuska. The Appellant argues that “Tokiwa already teaches a wiring layer connected to the solid state image pick up device 33,” and the ordinary artisan would not have reworked and replaced Tokiwa’s wiring layer and contacts with Kalliopuska’s bond wires as this would cause the signal paths to lengthen. Appeal Br. 5 (internal quotation mark omitted). The Appellant’s argument is not persuasive because it fails to address the Examiner’s fact finding and reasoning. As explained by the Examiner, the rejection is based on *replacing* Tokiwa’s solid state image pickup device 33 with a flip chip in view of Kalliopuska’s disclosure that “[f]lip chip bonding may be generally preferred as the signal paths between the sensor volume 202 and the read-out element 204 are kept short therewith.” Ans. 3–4 (quoting Kalliopuska ¶ 46).

The Appellant also argues that adding Kalliopuska’s bond wires would permanently connect Tokiwa’s sensor package 22 to contacts 41, 68 or wiring layer 24, thereby changing Tokiwa’s principle of operation by eliminating the image sensor’s modular nature and structure. *Id.* at 5–6. This argument is not persuasive because it is not supported by Tokiwa’s disclosure. More specifically, the Appellant has not refuted the Examiner’s finding that Tokiwa’s discussion of modularity relates to only the “freely attachable/detachable” connection of lens unit 4 to camera body 3. Ans. 4 (quoting Tokiwa ¶ 13). The Appellant has not presented arguments or evidence to refute the Examiner’s finding as to the advantages of wirebonds over the pressed contact terminals used by Tokiwa. *See* Ans. 4–5 (citing Tokiwa ¶ 29).

In sum, we are not convinced of reversible error in the Examiner’s obviousness rejection as to claims 1 and 8.

Claim 2 depends from claim 1 and requires that the image sensor comprise “an encapsulation layer that environmentally seals a surface of the PCB within the package substrate.” Appeal Br. 10 (Claims App.). Claim 9 depends from claim 8 and includes a similar limitation. *See id.* at 12. The Appellant argues that the Examiner reversibly erred in finding that Tokiwa discloses or suggests an encapsulation layer as claimed. Appeal Br. 7.

As to the claim 2 and claim 9 limitations, the Specification describes filling recess 12 with a dielectric encapsulation layer, such as resin encapsulation layer 52, and that “[t]he encapsulation layer may environmentally seal at least a surface of the PCB 20, the ROIC 42 and the PDA 46 within the package substrate 10.” Spec. ¶ 46. The Specification further discloses that encapsulation layer 52 may physically contact an optically transparent window or lid 48 attached to the upper surface of PDA 46 using, for example, a glass frit or another optically transparent adhesive. *Id.*

The Examiner found that Tokiwa describes covering mounting board 24 with attachment component 23. Ans. 6. The Examiner found that attachment component 23 “is sealed at the outer edges with the mount base 50 and at the inner edges with the glass cover 30 in order to create a seal enclosing the surface of the mounting board 24,” and “cover glass 30 of figure 7 of Tokiwa joins with the frame member 29 in order to seal the solid state image pickup device 33 to form the image sensor package 22.” *Id.* (citing Tokiwa ¶ 20). The Examiner further found that Tokiwa describes pressing image sensor package 22 toward attachment component 23 to create a seal along peripheral edge part 40 in attachment component 23 (*id.* (citing Tokiwa ¶ 21)), thereby “creat[ing] an enclosure that closes access to

air or moisture coming from the direction of the lens and thus forms an encapsulation layer environmentally sealing a surface of the mounting board 24” (*id.*).

Although the Specification describes the encapsulation layer as filling recess 12 (Spec. ¶ 46), the Appellant has not identified, nor do we find, any Specification disclosure that supports limiting claims 2 and 9 to an encapsulation layer having the specific structure described in Specification paragraph 46. The Appellant has not explained sufficiently why it was erroneous or unreasonable for the Examiner to find that Tokiwa’s Figure 7 and paragraphs 20 and 21 describe the claimed encapsulation layer that environmentally seals a surface of a PCB. *See* Appeal Br. 7 (arguing that Tokiwa’s attachment component 23 is not described as an encapsulation layer and “is at best a board” and that glass cover 30 seals only sensor 33).

Accordingly, we are not persuaded of reversible error in the Examiner’s rejection of claims 2 and 9.

Claim 3 depends from claim 2 and requires that the image sensor comprise “an electrical connector electrically coupled to the PCB, wherein the electrical connector extends from the circuit board through the encapsulation layer to provide an external package electrical connection to the PCB.” Appeal Br. 10 (Claims App.). Claim 10 depends from claim 9 and includes a similar limitation. *See id.* at 12. The Examiner determined that the ordinary artisan would have “form[ed] the solid state pickup device of Tokiwa with external leads extending from a leadframe as taught in Lee in order to provide an external electrical connection to the integrated circuit die.” Final Act. 6.

The Appellant argues that “[t]he leads of a lead frame as cited in Lee are not at all an electrical connector as the Applicant has claimed.” Appeal Br. 8. The Appellant argues that “[i]t is well understood in the art that electrical connections are not necessarily an electrical connector. Furthermore, the leads of a lead frame as taught by Lee would not and could not be reasonably combined with the other cited references to arrive at the Applicant’s claims.” *Id.*

The Specification discloses that “external package electrical connection to internal device electronics such as the PDA 46, the ROIC 42, and the PCB 20 may be performed using either first connector 26, second connector 30, or both.” Spec. ¶ 47. Figure 5 is described as depicting first connector 26 electrically coupled to PCB 20 and extending from a first device surface through encapsulation layer 52, thus providing an external package electrical connection to PCB 20. *Id.* Given this disclosure, the Examiner had a reasonable basis for finding that Lee teaches an electrical connector as recited in claims 3 and 10 “because [Lee’s leads] provide an electrical connection between the die and an external signal or power sources.” Ans. 6. The Appellant’s arguments to the contrary are not supported by persuasive evidence.

In sum, we are not convinced of reversible error in the Examiner’s rejection of claims 3 and 10.

As to the rejections of the remaining appealed claims, the Appellant contends that these claims are patentable for the same reasons argued in support of patentability of independent claims 1 and 8. *See* Appeal Br. 8. Because we do not find the Appellant’s arguments persuasive of reversible error in the Examiner’s rejection of claims 1 and 8, we also are not

persuaded of reversible error in the rejections of dependent claims 4, 5, 7, 11, 12, and 14–17.

DECISION SUMMARY

<b>Claims Rejected</b>	<b>35 U.S.C. §</b>	<b>Reference(s)/Basis</b>	<b>Affirmed</b>	<b>Reversed</b>
1, 2, 7–9, 14, 15	103	Tokiwa, Kalliopuska	1, 2, 7–9, 14, 15	
3, 10	103	Tokiwa, Kalliopuska, Lee	3, 10	
4, 5, 11, 12	103	Tokiwa, Kalliopuska, Kinsman	4, 5, 11, 12	
16	103	Tokiwa, Kalliopuska, Tseng	16	
17	103	Tokiwa, Kalliopuska, Shiu	17	
<b>Overall Outcome</b>			1–5, 7–12, 14–17	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED