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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte YAOJIAN LIN and SENG GUAN CHOW

Appeal 2019-005259
Application 15/169,095
Technology Center 2800

Before ROMULO H. DELMENDO, MICHAEL P. COLAIANNI, and CHRISTOPHER C. KENNEDY, *Administrative Patent Judges*.

DELMENDO, *Administrative Patent Judge*.

DECISION ON APPEAL

The Appellant[1] appeals under 35 U.S.C. § 134(a) from the Primary Examiner's decision to reject claims 1–4 and 6-26.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42—namely, "STATS ChipPAC Pte. Ltd." (Application Data Sheet filed May 31, 2016 at 5), which is also identified as the real party in interest (Appeal Brief filed February 11, 2019 ("Appeal Br.") at 1).

[2] *See* Appeal Br. 9–26; Reply Brief filed June 27, 2019 ("Reply Br.") at 1–17; Non-Final Office Action entered September 11, 2018 ("Non-Final Act.") at 9–21; Examiner's Answer entered May 2, 2019 ("Ans.") at 3–33.

I. BACKGROUND

The subject matter on appeal relates to a semiconductor device and its method of manufacture (Specification filed May 31, 2016 ("Spec.") ¶¶ 10–13). Claims 1, 8, 14, and 20, which are the only independent claims on appeal, are reproduced from the Claims Appendix to the Appeal Brief, as follows:

1. A method of making a semiconductor device, comprising:
providing a semiconductor die;
depositing an encapsulant around the semiconductor die;
disposing a first insulating layer over the semiconductor die and encapsulant;
forming a via in the first insulating layer over a contact pad of the semiconductor die;
disposing a first conductive layer over the first insulating layer and into the via;
disposing a second insulating layer over the first insulating layer and first conductive layer and further extending over the encapsulant; and
removing a portion of the second insulating layer to form an opening through the second insulating layer while retaining an island of the second insulating layer over a portion of the first conductive layer and extending across the via with a remaining portion of the second insulating layer after removing the portion of the second insulating layer to form the opening overlapping the first conductive layer and extending over the encapsulant, wherein a width of the island is greater than a width of the via and the island is off-center with respect to the opening in the second insulating layer.

8. A method of making a semiconductor device, comprising:
providing a semiconductor die;
disposing a first insulating layer over the semiconductor die;
forming a first via in the first insulating layer over a contact pad of the semiconductor die;
disposing a first conductive layer over the first insulating layer and into the first via;

disposing a second insulating layer over the first insulating layer and first conductive layer;

forming a second via in the second insulating layer over the first conductive layer and the first via with no portion of the second insulating layer remaining over the first via; and

disposing a second conductive layer over the first conductive layer and second insulating layer with an opening in the second conductive layer extending across the first via and further extending to the first conductive layer, wherein a width of the opening is greater than a width of the first via and the second conductive layer contacts the first conductive layer outside the first via and completely around the opening.

14. A semiconductor device, comprising:

a semiconductor die;

a first insulating layer disposed over the semiconductor die;

a via formed in the first insulating layer over a contact pad of the semiconductor die;

a first conductive layer disposed over the first insulating layer and in the via;

a second insulating layer disposed over a portion of the first insulating layer and first conductive layer; and

an opening formed through the second insulating layer to leave an island of the second insulating layer over a portion of the first conductive layer and extending across the via and a remaining portion of the second insulating layer overlapping the first conductive layer, wherein a width of the island is greater than a width of the via.

20. A semiconductor device, comprising:

a semiconductor die;

a first insulating layer disposed over the semiconductor die;

a first via formed in the first insulating layer over a contact pad of the semiconductor die;

a first conductive layer disposed over the first insulating layer and in the first via;

a second insulating layer disposed over the first insulating layer and first conductive layer;

> a second via formed in the second insulating layer over the first conductive layer and the first via with no portion of the second insulating layer remaining over the first via; and
>
> a second conductive layer disposed over the first conductive layer and second insulating layer with an opening in the second conductive layer extending across the first via and further extending to the first conductive layer, wherein a width of the opening is greater than a width of the first via and the second conductive layer contacts the first conductive layer outside the first via and completely around the opening.

(Appeal Br. 28–33).

II. REJECTIONS ON APPEAL

The Examiner maintains three rejections under AIA 35 U.S.C. § 103,[3] as follows:

A. Claims 1–4, 6, 7, and 26 as unpatentable over Kim et al.[4] ("Kim"), Lin et al.[5] ("Lin '070"), and Lin et al.[6] ("Lin '924");

B. Claims 8–13 and 20–25 as unpatentable over Ke et al.[7] ("Ke") and Wang et al.[8] ("Wang"); and

C. Claims 14–19 as unpatentable over Kim and Lin '070.

(Ans. 3–33; Non-Final Act. 9–21).

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[3] The Examiner states that a rejection under 35 U.S.C. § 112(b) of claims 8–13 and 20–25 has been withdrawn (Ans. 3).

[4] US 2013/0009286 A1, published January 10, 2013.

[5] US 2009/0079070 A1, published March 26, 2009.

[6] US 2013/0075924 A1, published March 28, 2013.

[7] US 2008/0182401 A1, published July 31, 2008.

[8] US 2011/0186987 A1, published August 4, 2011.

III. DISCUSSION

Rejections A & C. With respect to claim 1, the Examiner finds that Kim describes a method that includes some of the limitations recited in the claim but acknowledges numerous differences, as follows:

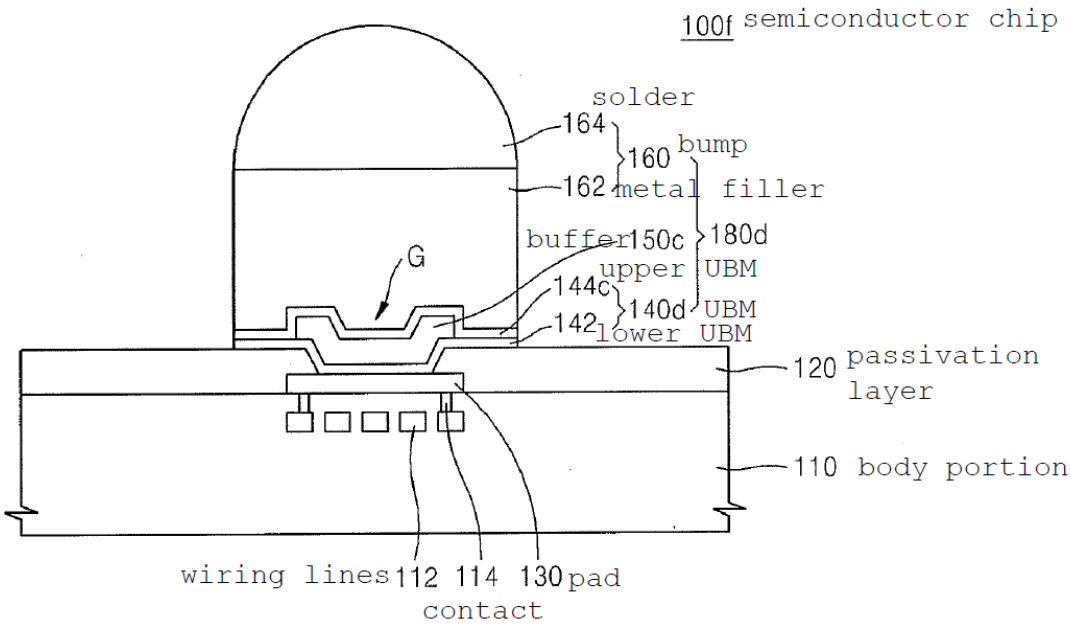
> Kim does not disclose, "Removing a portion of the second insulating layer to form an opening through the second insulating layer." "[Forming the opening] while retaining an island of the second insulating layer over a portion of the first conductive layer." "[The opening formed] with a remaining portion of the second insulating layer remaining after removing the portion of the second insulating layer to form the opening." "[The opening] overlapping the first conductive layer." . . .
>
> The combination of Kim and [Lin '070] does not disclose, "Depositing an encapsulant around the semiconductor die." "Disposing a first insulating layer over the semiconductor die and encapsulant." "[Disposing a second insulating layer over the] first conductive layer and further extending over the encapsulant." "[The opening] extending over the encapsulant." . . .
>
> The combination of Kim, [Lin '070], and [Lin '924] does not disclose, "The island is off-center with respect to the opening in the second insulating layer."

(Non-Final Act. 9–11). To bridge these gaps, the Examiner relies on Lin '070 and Lin '924 and the legal principle that where the general conditions are disclosed in the prior art, the discovery of optimum or workable ranges of a variable would have been obvious to a person having ordinary skill in the art (*id.*).

We agree with the Appellant (Appeal Br. 14–17) that the Examiner's rejection as maintained against claim 1 (and claims dependent thereon) is flawed because: (i) it fails to articulate sufficient reasons with some rational underpinning to support the conclusions that a person having ordinary skill in the art would have combined Kim, Lin '070, and Lin '924 in the manner

claimed, as required by *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)); and (ii) it fails to establish that the positioning of the "island . . . with respect to the opening in the second insulating layer," as recited in claim 1, is a result-effective variable, as required by controlling precedent such as *In re Applied Materials, Inc.*, 692 F.3d 1289, 1297 (Fed. Cir. 2012) (obviousness based on optimization of a variable requires a recognition in the prior art that the particular variable is result-effective). Our reasons follow.

Kim's Figure 9 (annotated) is reproduced, as follows:



Kim's Figure 9 above shows a semiconductor chip **100***f* including various elements as annotated (Kim ¶¶ 52, 56, 63, 83). As the Examiner acknowledges, Kim's method lacks many of the limitations recited in the "removing" step of claim 1, including the formation of islands of a second insulating layer.

Lin '070 does teach a semiconductor device that includes, e.g., passivation island **40** (Lin '070 ¶ 36; Fig. 6a). But the Examiner fails to

direct us to sufficient evidence or persuasive technical reasoning—i.e., some rational underpinning—establishing that Lin '070's teachings "would enhance the teachings of Kim" (Non-Final Act. 10). *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) ("'[C]onclusory statements' alone are insufficient and, instead, the finding must be supported by a 'reasoned explanation.'" (internal citation omitted)); *KSR*, 550 U.S. at 418 ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.").

Additionally, the Examiner's conclusion that a person having ordinary skill in the art would have "adjust[ed] the relative dimensions of the first conductive layer such that the island is not centered upon the first conductive layer so as to allow the position of the bump to be adjusted to the lower contact pad" (Non-Final Act. 11) also lacks evidentiary support or persuasive technical reasoning to support the notion that these variables would have been result-effective. *Applied Materials*, 692 F.3d at 1297.

Therefore, we do not sustain the rejection as maintained against claim 1 (and claims dependent thereon).

With respect to claim 14 (and claims dependent thereon), the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art . . . to combine the teachings of Kim with the teachings of [Lin '070] for the reasons provided above regarding claim 1" (Non-Final Act. 20). As we discussed above, however, the Examiner's rejection as maintained against claim 1 fails to articulate a sufficient reason with some rational underpinning to support a conclusion that a person having ordinary skill in the art would have combined the references in the manner claimed.

Therefore, we also do not sustain the rejection as maintained against claim 14 (and claims dependent thereon).

Rejection B. The Examiner finds that Ke describes some of the limitations recited in claim 8 but acknowledges numerous differences, as follows:

> Ke does not disclose, "[The opening] further extending to the first conductive layer." "[The second conductive layer contacts the first conductive layer] completely around the opening."
> . . . The combination of Ke and Wang does not disclose, "[Forming the second via] with no portion of the second insulating layer remaining over the first via."
> . . . The combination of Ke and Wang does not disclose, "[Disposing a second conductive layer] with an opening in the second conductive layer extending across the first via." "Wherein a width of the opening is greater than a width of the first via."
> . . . The combination of Ke and Wang does not disclose, "The second conductive layer contacts the first conductive layer outside the first via."

(Non-Final Act. 13–15). To account for these gaps, the Examiner relies on Wang and obviousness based on optimization and rearrangement of parts (*id.*).

But this rejection, like Rejections A and C, lacks a sufficient articulated reason for combining the references in the manner claimed. Ke describes a method for making a semiconductor device having, *inter alia*, openings **36** that are shifted in position from the center of a corresponding one of bonding pads **31** by a predetermined distance **S** (Ke ¶¶ 46–49; Figs. 3A-3F). Wang, by contrast, discloses a different semiconductor device **800** including a semiconductor substrate **802**, a top metal layer **804**, first passivation layers **806**, a bonding pad **808**, passivation layers **810**, stress

buffer structures **812**, and UBM (under bump metallization) structures **814** (Wang ¶ 66; Fig. 8C).

We have not been directed to any evidence or persuasive technical reasoning to support the conclusion that some of the elements taught in Wang "would enhance the teachings" of Ke (Non-Final Act. 14). For this reason, the rejection as maintained against claim 8 (and claims dependent thereon) cannot be sustained. *NuVasive, Inc.*, 842 F.3d at 1383; *KSR*, 550 U.S. at 418.

Claim 20 has been rejected on the same basis (Non-Final Act. 17). Therefore, we also cannot sustain the rejection of claim 20 (and claims dependent thereon).

IV. CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–4, 6, 7, 26	103	Kim, Lin '070, Lin '924		1–4, 6, 7, 26
8–13, 20–25	103	Ke, Wang		8–13, 20–25
14–19	103	Kim, Lin '070		14–19
Overall Outcome				1–4, 6–26

REVERSED