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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DAVIDE GIUSEPPE PATTI, MONICA MICCICHÉ, ANTONIO GIUSEPPE GRIMALDI, ANGELA LONGHITANO, and SALVATORE LIOTTA

Appeal 2019-004759
Application 14/028,364
Technology Center 2800

Before BEVERLY A. FRANKLIN, LINDA M. GAUDETTE, and MONTÉ T. SQUIRE, *Administrative Patent Judges.*

GAUDETTE, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

The Appellant[2] appeals under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 8–18, 21, and 22 under 35 U.S.C. § 103(a) over Takano (US 2004/0041207 A1, pub. March 4, 2004) in view of

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[1] This Decision includes citations to the following documents: Specification filed September 16, 2013 ("Spec."); Final Office Action dated June 11, 2018 ("Final"); Appeal Brief filed December 14, 2018 ("Appeal Br."); Examiner's Answer dated March 28, 2019 ("Ans."); and Reply Brief filed May 24, 2019 ("Reply Br.").

[2] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42. The Appellant identifies the real party in interest as STMicroelectronics S.r.1. Appeal Br. 2.

Suekawa (US 2012/0132912 A1, pub. May 31, 2012) and Ohtomo (US 6,835,615 B2, iss. December 28, 2004).[3]

We AFFIRM.

CLAIMED SUBJECT MATTER

The invention "relates to vertical gate MOS field effect transistors." Spec. 1:5–6. The invention is illustrated in Figure 1, reproduced below

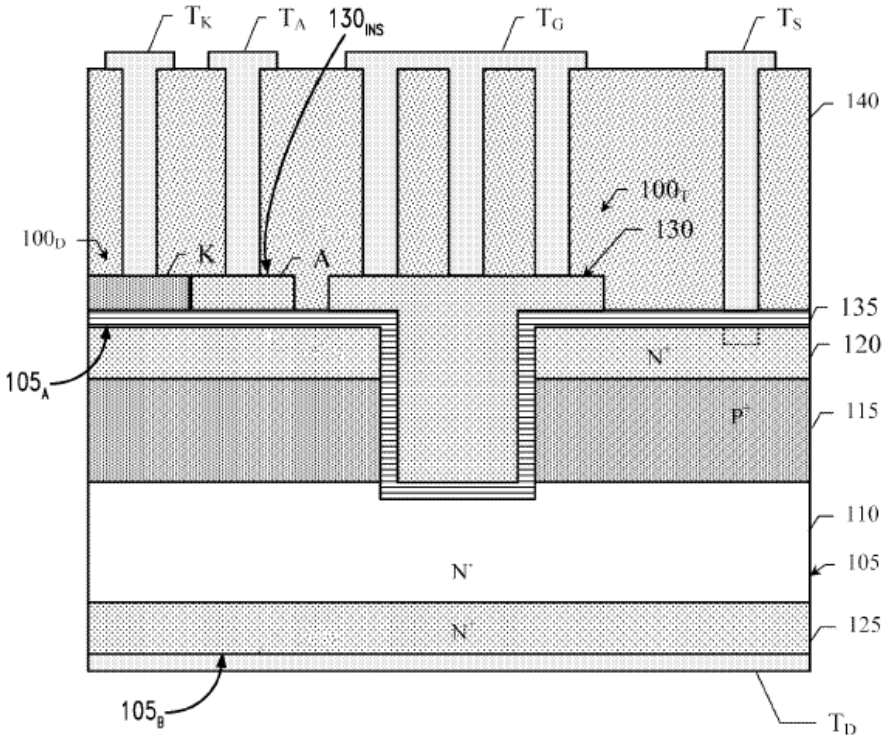


FIG. 1

Figure 1 is a sectional view of an electronic device comprising transistor 100_T and thermal diode 100_D, integrated on chip 105. Spec. 4:7–9, 16. Transistor 100_T comprises drain region 125, N^--type drift region 110, P^+-

[3] We have jurisdiction under 35 U.S.C. § 6(b).

type body region 115, N^+-type source region 120, and gate region 130. *Id.* at 4:19–22, 25–26. Gate region 130 extends vertically through source region 120 and body region 115, and into drift region 110. *Id.* at 4:25–5:1. Insulating layer 135 electrically insulates gate region 130 from chip 105. *Id.* at 5:1–2. Insulating layer 135 also insulates thermal diode 100_D's anode region A and cathode region K from chip 105. *Id.* at 5:4–8.

Claim 8, reproduced below, is illustrative of the claimed subject matter:

> 8. An electronic device, comprising:
>
> a semiconductor substrate;
>
> a vertical trench MOS transistor in the semiconductor substrate, the MOS transistor including:
>
> a body region extending in the semiconductor substrate from a main surface of the semiconductor substrate, the body region having a first type of conductivity;
>
> a source region extending in the body region from the main surface, the source region having a second type of conductivity;
>
> a gate region of conductive material extending in the semiconductor substrate from the main surface through the body region;
>
> a continuous insulating layer between the gate region and the semiconductor substrate;
>
> a thermal diode adjacent to the gate region, the thermal diode including:
>
> *an anode region directly overlying the source region*, the anode region being spaced from the source region by the continuous insulating layer, *the continuous insulating layer being in contact with the gate region and the anode region, the continuous insulating layer being continuous between the gate region and the anode region*; and

> *a cathode region directly overlying the source region*, the cathode region being spaced from the source region by the continuous insulating layer; and
>
> a dielectric layer separating the gate region from the anode region of the thermal diode, a portion of the dielectric layer being in contact with the gate region, the continuous insulating layer, and the anode region of the thermal diode.

Appeal Br. 22 (Claims Appendix).

OPINION

The Examiner found that Takano discloses an electronic device comprising "a semiconductor substrate" and "a vertical trench MOS transistor" having the features recited in claim 8, as well as "a continuous insulating layer between the [MOS transistor's] gate region and the semiconductor substrate" (claim 8). Final 7. The Examiner determined that the ordinary artisan would have modified Takano's device to include Suekawa's thermal diode and Ohtomo's dielectric layer

> to have the predictable result of being able to accurately measuring temperature in [the] immediate vicinity of high density current without interfering with normal operation which would allow for prevention of device destruction due to high heat . . . , and in order to have the predictable result of passivating the upper surface of the device and protect the device from processing conditions during electrode formation, respectively.

Id. at 9–10. The Examiner determined that these modifications to Takano's device would have resulted in the claim 8 electronic device. *See generally id.* at 7–10.

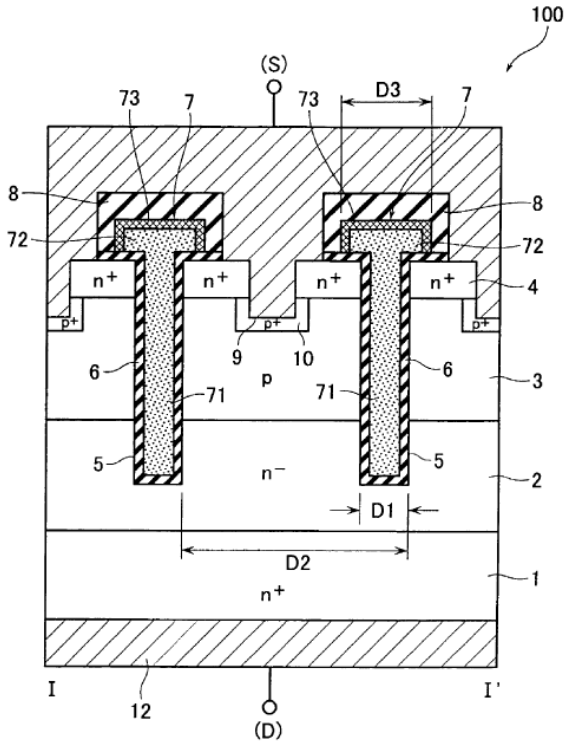
The Appellant contends the Examiner reversibly erred in determining that the combination of Takano, Suekawa, and Ohtomo would have suggested a device in which (1) the thermal diode anode and cathode regions

directly overlie the source region, and (2) the continuous insulating layer is in contact with, and continuous between, the gate region and the anode region. Appeal Br. 15, 20; *see supra* claim 8 italicized language. The Appellant's arguments are not persuasive of reversible error for the reasons explained in the Final Office Action and in the Answer. We add the following to address the arguments made by the Appellant in the Reply Brief.

Suekawa discloses MOSFET chip 100 comprising source electrode 101, gate pad 102, and temperature sensing diode 120 that detects chip temperature. Suekawa ¶¶ 28, 73, Fig. 14. Temperature sensing diode 120 comprises anode electrode 121 disposed on p-type polysilicon 123 via barrier metal layer 9, and cathode electrode 122 disposed on n-type polysilicon 124 via barrier metal layer 9. *Id.* ¶ 74, Fig. 15. Temperature sensing diode 120 is disposed on silicon oxide film 11. *Id.* ¶ 74.

Takano discloses a trench gate type semiconductor device. Takano Figure 2, reproduced below, illustrates "a power MOS transistor 100 in accordance with one embodiment of the invention." Takano ¶ 26.

FIG. 2



Takano Figure 2 is a cross-sectional view of power MOS transistor 100 comprising drain layer 1, n^--type layer 2, p-type layer layer 3, N^+-type source layer 4, and gate electrode 7. Takano ¶¶ 26–27. Gate electrode 7 is formed in trench 5 that extends vertically through source layer 4 and p-type base layer 3, and into n^--type layer 2. *Id.* ¶ 33. Insulator film 6 overlies trench 5's bottom surface and sidewall. *Id.* ¶ 35. "[G]roove 9 which reaches p-base layer 3 from source layer 4 is formed in each unit cell region laterally interposed between gate electrode 7." *Id.* ¶ 30. The source electrode is buried in groove 9 and, therefore, in contact with source layer 4 and base layer 3. *Id.* Takano describes a fabrication process for MOS transistor 100 with reference to Figures 3–12. *Id.* ¶ 32.

The Appellant argues that the Examiner failed to support a finding that in a device resulting from the combination of Takano and Suekawa, the thermal diode would directly overlie the source layer. Reply Br. 2. The

Appellant reiterates the argument advanced in its Appeal Brief (*see* Reply Br. 2) that if the ordinary artisan were to modify Takano's device to include Suekawa's thermal diode 120, such person "would position the diode 120 of Suekawa lateral to the transistor 100 of Takano" such that the thermal diode's anode and cathode regions would not directly overlie the source region as required by claim 8, "because the only teaching in the three references regarding the positioning of a thermal diode is Suekawa's teaching to position the diode 120 laterally to the source region 4" (Appeal Br. 17). The Appellant further argues that Takano describes removing portions of source layer 4 to form grooves and does not suggest any reason to retain source layer 4 in any regions other than those shown in Takano Figure 2. *See* Reply Br. 2.

The Appellant's arguments are not persuasive of reversible error because they are directed to Takano's and Suekawa's individual teachings, and fail to identify error in the Examiner's findings as to what the collective teachings of the prior art would have suggested to one of ordinary skill in the art. *See* Ans. 3–4; *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991). In the Final Office Action, the Examiner explained that addition of a thermal diode to Takano's device would occur during the method steps of modifying Takano's Figure 7 structure to achieve Takano's Figure 8 structure. Final 8. Takano Figure 7 illustrates the structure after deposition of insulator film 6, followed by deposition of polysilicon layer 71 on source layer 4 so as to completely bury trench 5 and make the structure's top surface substantially flat. Takano ¶ 35. Takano Figure 8 illustrates the structure after etching polysilicon layer 71 to form gate electrode 7 having a T-shaped profile. *Id.* ¶ 36. The Examiner found that the ordinary artisan would have used a

portion of polysilicon layer 71 deposited on source layer 4, as shown in Takano Figure 7, to form a thermal diode as described in Suekawa. Final 8–9; *see also* Suekawa ¶ 75 (stating that the thermal diode is formed in the same process as source electrode 101 and gate pad 102). The Examiner found that in the resultant structure, the thermal diode's anode and cathode regions would directly overlie the source region, and be spaced from the source region by insulating film 6, i.e., a continuous insulating layer as claim 8 requires. *Id.* at 9. The Appellant has not persuasively explained why these findings, as well as the Examiner's findings as to why the ordinary artisan would have modified Takano to include Suekawa's thermal diode (*see* Final 9–10) are erroneous or unreasonable.

The Appellant argues that the Examiner failed to address sufficiently the Appellant's argument that Takano's device, as modified to include Suekawa's thermal diode, would not function as intended absent major redesign. Reply Br. 2. In the Appeal Brief, the Appellant argues that if one of Takano's unit cells were modified to retain dielectric layer 6 over the entire surface for the purpose of incorporating a thermal diode as proposed by the Examiner, that unit cell would no longer function as intended because source electrode 11 would not contact base layer 3 and source layer 4. Appeal Br. 21; *see* Takano Fig. 2, ¶ 30 (source electrode is buried in groove 9 and in contact with source layer 4 and base layer 3). The Examiner responds that the benefit of being able to accurately determine the device's operating temperature would outweigh any drawbacks in eliminating one out of hundreds of contact areas between source electrodes and source layer 4. Ans. 4–5.

We find the Examiner's evidence and reasoning sufficient to support a finding that the ordinary artisan would have modified a unit cell to incorporate a thermal diode and would have had a reasonable expectation of success in so doing. The burden, therefore, was properly shifted to the Appellant to show the contrary. The Appellant has not met this burden because the Appellant has not identified persuasive evidence to support its arguments that Takano's device would no longer function as intended or that the ordinary artisan would have been dissuaded from making the proposed modification to avoid losing the functionality of a unit cell as a vertical transistor. *See* Reply Br. 3; *In re Urbanski*, 809 F.3d 1237, 1243 (Fed. Cir. 2016) ("In cases involving mechanical device or apparatus claims, we have held that '[i]f references taken in combination would produce a "seemingly inoperative device," . . . such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness.'" (quoting *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1354 (Fed. Cir. 2001))).

In sum, for the reasons stated in the Final Office Action, the Answer, and above, the Appellant's arguments are not persuasive of reversible error in the Examiner's conclusion of obviousness.

DECISION SUMMARY

Claims Rejected	**35 U.S.C. §**	**Reference(s)/Basis**	**Affirmed**	**Reversed**
8–18, 21, 22	103(a)	Takano, Suekawa, Ohtomo	8–18, 21, 22	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED