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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte YASUHIRO TAKAI

Appeal 2019-004481
Application 14/947,122
Technology Center 2800

Before ADRIENE LEPIANE HANLON, KAREN M. HASTINGS, and DEBRA L. DENNETT, *Administrative Patent Judges*.

DENNETT, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[2] appeals from the Examiner's decision to reject claims 7–12 of Application 13/956,054, which constitute all the claims pending in this application. We have jurisdiction under 35 U.S.C. § 6(b).

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[1] In our Decision, we refer to the Specification ("Spec.") of Application No. 14/947,122 filed Nov. 20, 2015; the Final Office Action dated May 22, 2018 ("Final Act."); the Appeal Brief filed Feb. 8, 2019 ("Appeal Br."); the Examiner's Answer dated Mar. 14, 2019 ("Ans."); and the Reply Brief filed May 14, 2019 ("Reply Br.").

[2] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Micron Technology, Inc. Appeal Br. 3.

For the reasons set forth below, we AFFIRM.

The subject matter of the invention relates to improving access speed in input receiver circuits of semiconductor devices. Spec. ¶ 2. The invention accomplishes improved access speed by use of a capacitor for pre-emphasis. Spec. ¶ 30. The capacitor accelerates a rise of the signal of a node and a discharge operation at another node, resulting in faster signal propagation of the input receiver circuit. Spec. ¶ 31.

FIG. 1 of the '122 Application is reproduced below:

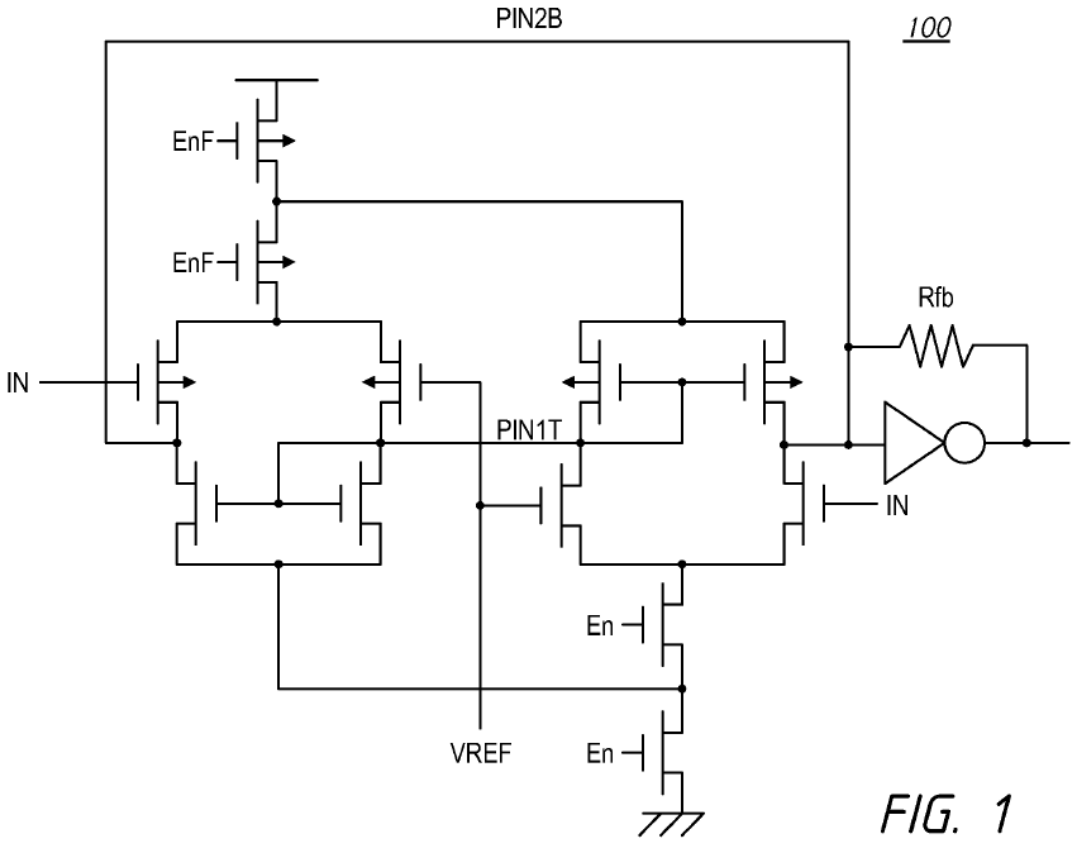

FIG. 1
(Prior Art)

FIG. 1 (labeled Prior Art) is a circuit diagram of an example of a quad-coupled receiver (QCR) type input receiver circuit. Spec. ¶ 8. FIG. 3 of the '122 Application, which illustrates an embodiment of the claimed invention, differs from FIG. 1 in that input receiver circuit 300 in FIG. 3

(similar to input receiver circuit 100 in FIG. 1) includes a capacitor (Cpre) coupled between the input node (IN) and a third node (PIN1T) that is not disclosed in FIG. 1. *Id.* ¶ 30.

FIG. 3 of the '122 Application is reproduced below:

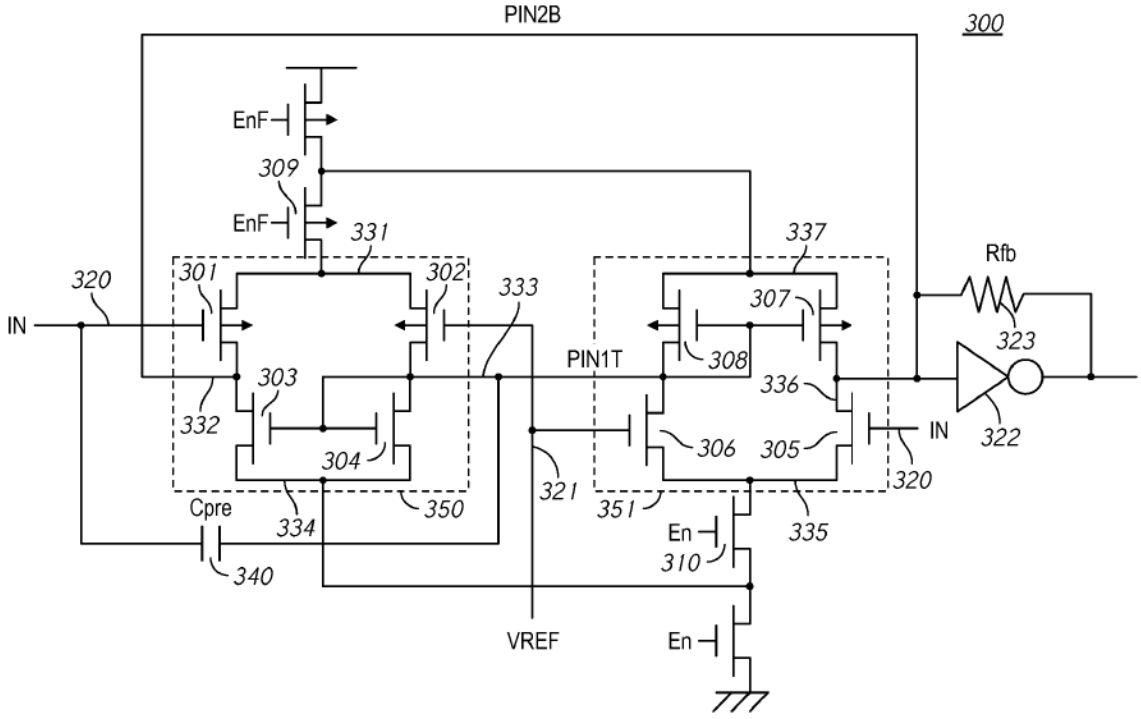

FIG. 3

FIG. 3 is a circuit diagram of an example of an input receiver circuit according to an embodiment of the claimed invention. Spec. ¶ 27; *see also* Appeal Br. 3–4. Input receiver circuit 300 includes input node 320 that is supplied with an input signal and reference node 321 that is supplied with a reference voltage VREF. Spec. ¶ 27. Input receiver circuit 300 also includes first amplifier circuit 350 and second amplifier circuit 351, each including a plurality of transistors. *Id.* ¶¶ 27, 28. Input receiver circuit 300 includes transistors to which ground voltage VSS and positive voltage VDD are supplied. *Id.* ¶ 29. Ninth transistor 309 is coupled between first node 331 and seventh node 337 and has a gate coupled to a complementary signal

of an activation signal, and tenth transistor 310 is coupled between the fourth node and the fifth node and has a gate coupled to the activation signal. *Id.* The activation signal may be provided to enable or disable the input receiver circuit 300. *Id.*

Input receiver circuit 300 may also include inverter 322 and feedback resistor 323. *Id.* Inverter 322 receives a signal from sixth node 336 and in response, provides an output signal to the output node. *Id.* Feedback resistor 323 is coupled between sixth node 336 and the output node for suppressing amplitude of a signal at second node 332 (PIN2B) that helps the circuit to transmit the output signal with very high speed. *Id.*

Input receiver circuit 300 differs from the QCR type input receiver circuit in FIG. 1 (labeled as "Prior Art" by the inventor) in that input receiver circuit 300 also includes capacitor (Cpre) 340 coupled between input node 320 and third node 333 for pre-emphasis, i.e., capacitively coupling transitions in the input voltage to the third node 333, which may assist changing a voltage of the third node 333. *See id.* ¶ 30, FIG. 1. Transition of the input signal at input node 320 causes a one-shot pulse of pre-emphasis on third node 333. *Id.*

> For example, when the input signal becomes active and a signal level of the input node 320 becomes a logic high, the first transistor 301 and the fifth transistor 305 receive the active input signal which causes a signal level of the second node (PIN2B) 332 to become a logic low. At the same time, a high-pulse signal of the third node (PIN1T) 333 decreases capability of the seventh transistor 307 and the eight transistor 308 sharing the third node (PIN1T) 333 and increases capability of the third transistor 303 and the fourth transistor 304 where the third, fourth, seventh and eighth transistors, 303, 304, 307, and 308 share the third node (PIN1T) 333. The decrease of the capability of the seventh transistor 307 and the eighth transistor 308 and the increase of the capability of the third transistor 303 and the fourth transistor

> 304 may assist the signal level of the second node (PIN2B) 332 to transition to a logic low.

Id.

Claim 1, reproduced below from the Claims Appendix of the Appeal Brief with disputed limitations italicized, illustrates the claimed subject matter:

> 1. An apparatus comprising:
>
> an input node;
>
> a reference node supplied with a reference voltage;
>
> first, second, third, fourth, sixth, and seventh nodes;
>
> a first transistor coupled between the first node and the second node, the first transistor having a gate coupled to the input node;
>
> a second transistor coupled between the first node and the third node, the second transistor having a gate coupled to the reference node;
>
> a third transistor coupled between the second node and the fourth node, the third transistor having a gate coupled to the third node;
>
> a fourth transistor coupled between the third node and the fourth node, the fourth transistor having a gate coupled to the third node;
>
> a seventh transistor coupled between the sixth node and the seventh node, the seventh transistor having a gate coupled to the third node;
>
> an eighth transistor coupled between the third node and the seventh node, the eighth transistor having a gate coupled to the third node;
>
> a ninth transistor coupled between the first node and the seventh node, wherein only a single transistor is connected between the first node and the seventh node;

> a tenth transistor coupled between the fourth node and the fifth node, wherein only a single transistor is connected between the fourth node and the fifth node;
>
> an eleventh transistor coupled to the seventh node;
>
> a twelfth transistor coupled to the fourth node; and
>
> *a capacitor coupled between the input node and the third node*,
>
> *wherein only a single capacitor is connected between the input node and all of the third transistor, the fourth transistor, the seventh transistor, and the eighth transistor*, and
>
> wherein a transition of input signal at the input node causes a pulse of pre-emphasis on the third node.

REFERENCE

The Examiner relies on U.S. Patent No. 7,859,916 B2 to Amirabadi, issued Dec. 28, 2010 ("Amirabadi") in conjunction with FIG. 1 of the '122 Application in rejecting the claims. Final Act. 2.

REJECTIONS

The Examiner maintains the rejection of claims 1–6, 8–12, and 19–21 under 35 U.S.C. § 103(a) as obvious over FIG. 1 of the '122 Application ("AAPA") in view of Amirabadi's Figure 1. Final Act. 2–6.

DISCUSSION

We review the appealed rejections for error based upon the issues identified by Appellant and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential), (cited with approval in *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011)) ("[I]t has long been the Board's practice to require an applicant to identify the alleged error in the [E]xaminer's rejections.").

Appellant argues the three independent claims (claims 1, 11, and 21) separately, and relies on the arguments made in relation to the independent claims to support patentability of the claims depending therefrom. *See* Appeal Br. 7–16.

Claim 1

The Examiner rejects claim 1 over the combination of FIG. 1 of the '122 (which the Examiner references as Applicant's admitted prior art, "AAPA") in view of Amirabadi Figure 1. Final Act. 2–4. The Examiner finds that AAPA discloses the limitations of claim 1 except for "a capacitor coupled between the input node and the third node." *Id.* at 3.

The Examiner relies on Amirabadi Figure 1 to teach the claimed capacitor. *Id.* Amirabadi Figure 1 is reproduced below with capacitors C1 and C2 identified by bold lines and arrows to aid in our discussion:

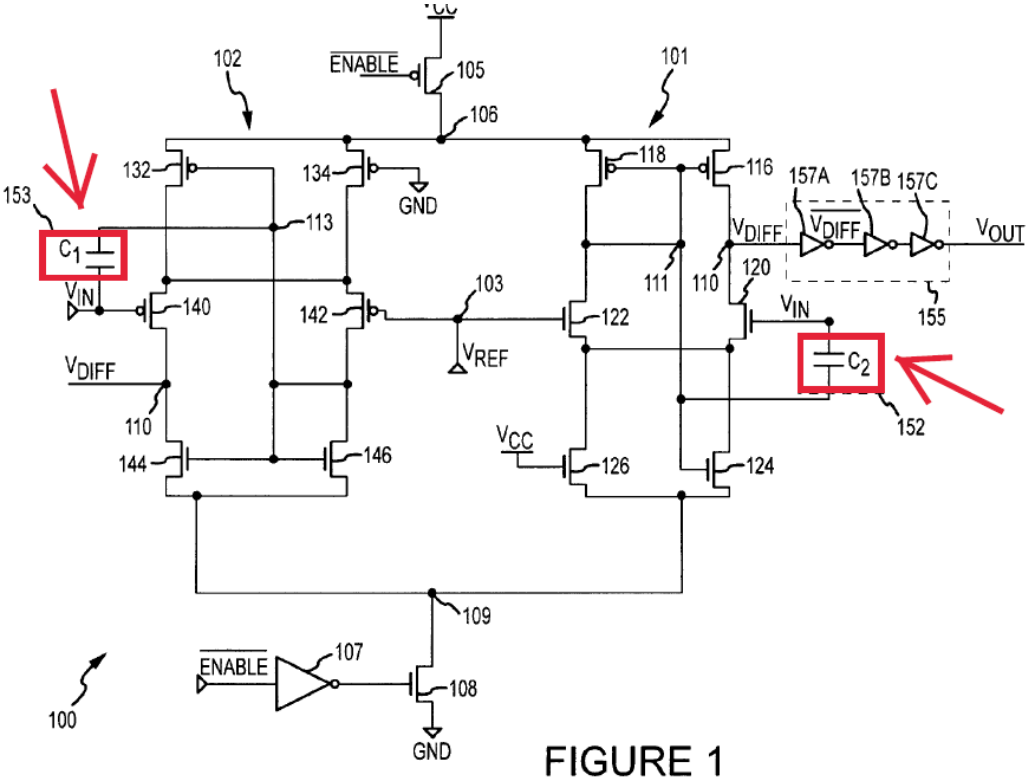

FIGURE 1

Amirabadi Figure 1 is a schematic of a differential input buffer circuit according to an embodiment of Amirabadi's invention. Amirabadi col. 1, ll. 61–62. Amplifier 101 (on right side of figure) includes capacitively coupling the gate of transistor 120 to the gates of transistors 116, 118, 124 at node 111 by coupling capacitor 152 (C2). *Id.* col. 1, l. 65–col. 2, l. 1. Amplifier 102 (on left side of figure) includes capacitively coupling the gates of transistors 132, 144, 146 at node 113 by coupling capacitor 153 (C1). *Id.* col. 2, ll. 1–5. Capacitors 152 and 153 couple transitions of the input signal V_{IN} to nodes 111 and 113, respectively. *Id.* col. 2, ll. 5–7. This capacitive coupling makes amplifiers 101 and 102 operate in a substantially symmetrical manner because they mimic the operation of amplifiers 101 and 102 as if complementary signals were applied to the amplifiers. *Id.* col. 2, ll. 8–12.

The Examiner finds that Amirabadi's Figure 1 shows a circuit similar to AAPA, but having two capacitors, C1 and C2, coupled between the input node and nodes 113 and 111, respectively. Ans. 3–4. The Examiner provides an annotated, modified version of AAPA after modifying AAPA with Amirabadi's capacitors to illustrate the finding:

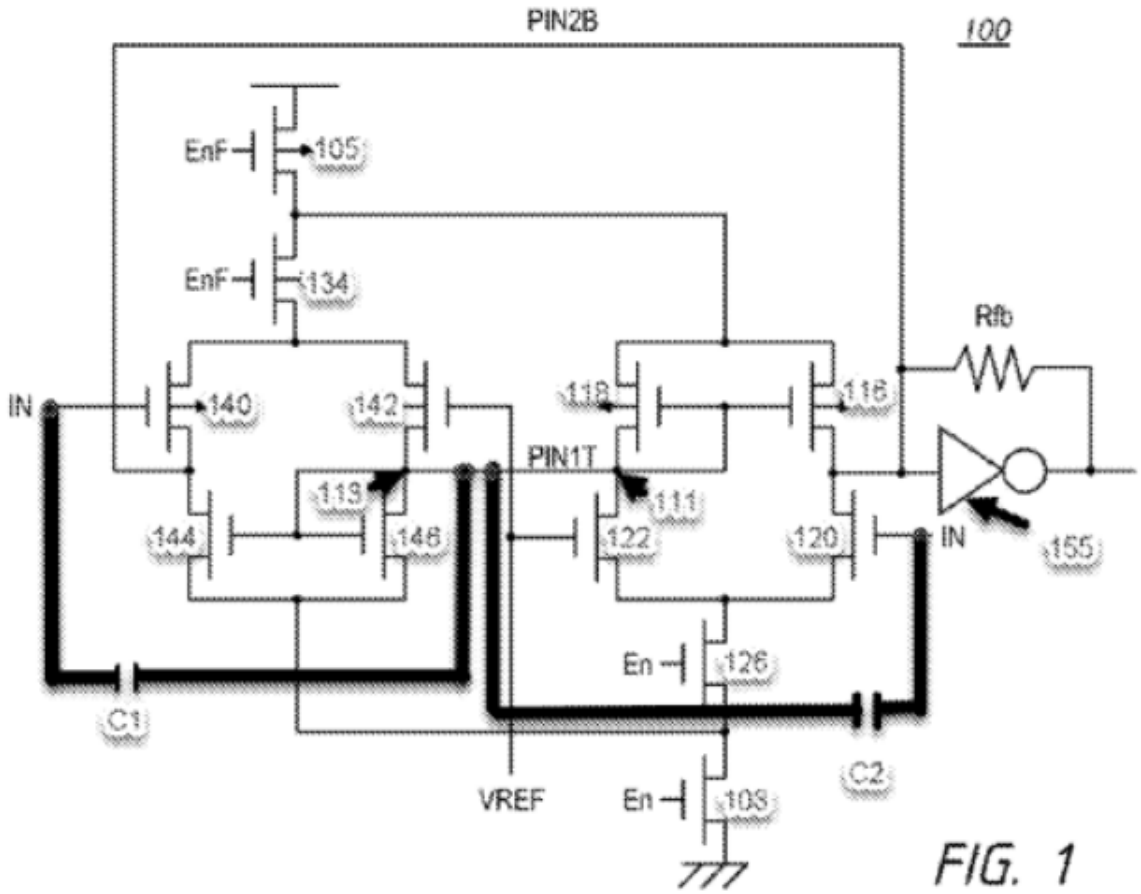

FIG. 1
(Prior Art)
after being modified

As initially modified by the Examiner, the figure shows the addition of capacitors C1 and C2 in bold black lines. *See* Ans. 4.

The Examiner determines that it would have been obvious to one of ordinary skill in the art to add Amirabadi's capacitors to AAPA for the purpose of reducing noise. *Id.*

The Examiner finds that nodes 111 and 113 are equivalent to AAPA third node (333/ PIN1T in Figure 3 *supra*). *Id.* The Examiner finds that in modified AAPA, capacitors C1 and C2 are connected in parallel. *Id.* According to the Examiner, it was well known that parallel connected capacitors are equivalent to a single capacitor having a capacitance equal to

the sum of capacitances of the parallel connected capacitors. *Id.* Therefore, the Examiner concludes that it would have been obvious to use a single capacitor—Ct—for capacitors C1 and C2 for the purpose of saving space. *Id.* at 5. The Examiner illustrates the point with a further modified version of AAPA:

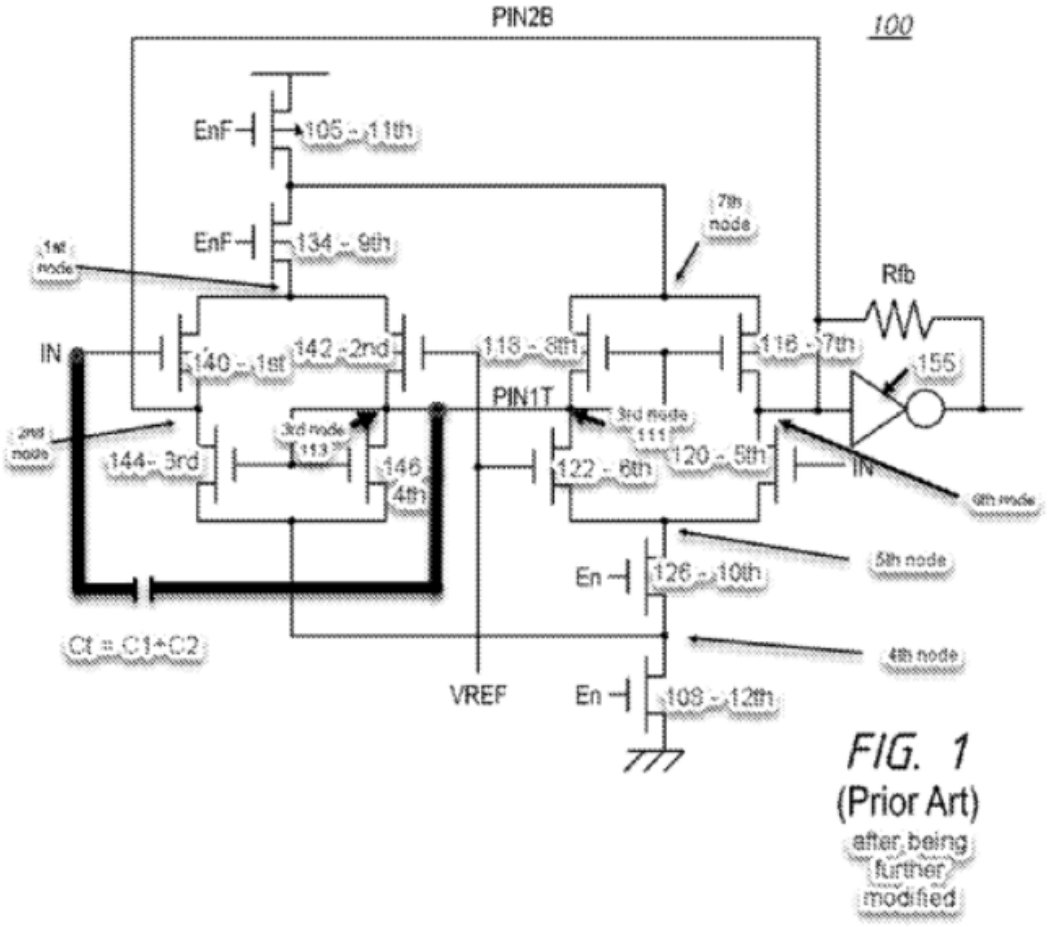

FIG. 1
(Prior Art)
after being further modified

As further modified by the Examiner, the figure shows capacitor Ct in place of capacitors C1 and C2. *Id.* Based on this further modification of AAPA, the Examiner finds that AAPA in view of Amirabadi teaches, "a capacitor coupled between the input node and the third node." *Id.*

Appellant argues that AAPA does not illustrate a connection between the input node and the common node, let alone a capacitor connecting them. Appeal Br. 8. Appellant argues Amirabadi's gates of PMOS transistors 116

and 118 of amplifier 101 are not connected to the gates of NMOS transistors 144 and 146 of amplifier 102, and the input buffer operates with two capacitors, not only a single capacitor. *Id.* Appellant argues that Amirabadi's input buffer does not include a node that is common to the PMOS and NMOS transistors of the respective amplifiers 101 and 102, thus does not disclose the claimed features. *Id.* at 9.

These arguments by Appellant are not persuasive because they attack the references individually. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). Each reference cited by the Examiner must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole. *See id.* Appellant's arguments do not address the proposed modification, thus fail to rebut the Examiner's findings.

Appellant acknowledges that the difference between claim 1 and FIG. 1 of the '481 Application—identified by the applicant as prior art—is the presence of capacitor Cpre. *See* Spec. ¶ 30. The Examiner combines the circuit shown in FIG. 1 of the '481 Application (AAPA) with capacitors from Amirabadi, putting them between AAPA's input node and the third node. *See* Final Act. 3. The Examiner concludes that the inclusion of capacitor(s) would reduce noise (*id.*), which qualifies as "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" to support the combination. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). Appellant does not explain why the reason articulated by

the Examiner for combining the references is erroneous or unreasonable. *See id.*

Appellant also argues that Amirabadi teaches away from claim 1. Appeal Br. 9. Appellant contends that Amirabadi discloses a symmetrical topography of differential amplifiers that causes them to operate in a symmetrical manner when they receive complementary signals. *Id.* According to Appellant, removing one of capacitors 152 and 153 means that Amirabadi's differential amplifiers would not operate in a symmetrical manner when they receive complementary signals, which defeats the primary purpose of Amirabadi's input buffer circuit. *Id.*

The appropriate inquiry when considering whether a reference teaches away is whether the reference "criticize[s], discredit[s], or otherwise discourage[s] the solution claimed" by Appellant. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Nothing in Amirabadi criticizes, discredits, or otherwise discourages the use of a capacitor in AAPA—and Appellant does not argue to the contrary. *See* Appeal Br. 8. Appellant's argument concerns what the consequences of changing the capacitors in Amirabadi would do to *Amirabadi's* circuit, not to the circuit of AAPA as modified by the Examiner. Thus, this argument is unpersuasive of reversible error.

In the Reply Brief, Appellant argues, "Amirabadi discloses a self-bias type input buffer circuit, which is a completely different circuit than the bias-type input buffer circuit of AAPA." Reply Br. 2. Appellant argues that Amirabadi's circuit includes transistors 124 and 132 that are turned on by nodes 111 and 113, respectively, and transistors 124 and 132 are coupled as pairs with transistors 126 and 134, respectively. *Id.* Appellant argues that instead of using a single transistor to power each amplifier circuit, Amirabadi's amplifiers include two transistors each (transistors 124 and 126

for amplifier 101 and transistors 132 and 134 for amplifier 102). *Id.* at 2–3. Appellant contends that Amirabadi fails to disclose, "wherein only a single capacitor is connected between the input node and all of the third transistor, the fourth transistor, the seventh transistor, and the eighth transistor, as recited in claim 1." *Id.* at 3.

In these arguments, Appellant again addresses one reference individually, rather than the modification of AAPA by Amirabadi proposed by the Examiner. *See Merck*, 800 F.2d at 1097. As such, the arguments do not rebut the Examiner's findings, which depend on combining Amirabadi's capacitors with AAPA's circuit, and do not rely on modifying Amirabadi's circuit. *See* Final Act. 2–4; Ans. 3–7. The Examiner's modified circuit comprises "only a single capacitor is connected between the input node and all of the third transistor, the fourth transistor, the seventh transistor, and the eighth transistor, as recited in claim 1." *See* Ans. 5.

In the Examiner's modification, the capacitors are coupled in parallel, and then combined to be a single capacitor. *See id.* at 4–5. Appellant argues that Amirabadi's capacitors are not coupled in parallel, and suggests that modifying AAPA with Amirabadi would result in a circuit with two capacitors coupled to two corresponding nodes. Reply Br. 4.

However, it is well established that the obviousness inquiry does not ask "whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole." *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc); *see also In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (stating "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference"); *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) ("Combining the *teachings* of

references does not involve an ability to combine their specific structures."). To justify combining reference teachings in support of a rejection it is not necessary that a device shown in one reference can be physically inserted into the device shown in the other. *Keller*, 642 F.2d at 425. Thus, Appellant imposes a burden on the Examiner that is greater than the law requires. We are satisfied that the Examiner has shown sufficient reason why one of ordinary skill in the art would combine the references in the manner proposed and that such a skilled artisan, being a person of ordinary creativity and not an automaton, would have been able to make the necessary adjustments and further modifications to result in a properly functioning device. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ").

> Such a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. . . . When a work is available in one field, design incentives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, § 103 likely bars its patentability. Moreover, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill. A court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 416.

For the reasons above, we determine that the Examiner did not reversibly err in rejecting claim 1 as unpatentable over AAPA in view of

Amirabadi. Accordingly, we also affirm the rejection of dependent claims 2–6, and 8–10. 37 C.F.R. § 41.37(c)(1)(iv).

Claim 11

Claim 11 is drawn to an apparatus having components similar to that of claim 1, and recites the following limitations in which the disputed terms are italicized:

> 11. An apparatus, comprising:
>
> a ninth transistor coupled between the first node and the seventh node, *wherein only a single transistor is connected between the first node and the seventh node*;
>
> a tenth transistor coupled between the fourth node and the fifth node, *wherein only a single transistor is connected between the fourth node and the fifth node*;
>
> . . .
>
> *wherein the ninth transistor has a gate configured to receive a first bias signal and the tenth transistor has a gate configured to receive a second bias signal, wherein the first bias signal and the second bias signal are generated externally and supplied to the gate of the ninth transistor and the gate of the tenth transistor*, ...

Appeal Br. 19–20 (Claims App'x).

FIG. 6 of the '481 Application illustrates the embodiment claimed in claim 6. *See* Appeal Br. 4–6; Spec. ¶¶ 32–35. According to the Specification, the input receiver circuit in FIG. 6 differs from the QCR type input receiver in FIG. 3 (which illustrates claim 1) by including a second capacitor (CpreN) and nodes for receiving bias signals. Spec. ¶¶ 33–34.

The Examiner finds that Figure 1 of Amirabadi shows signals Vcc and GND that are provided by circuits that are not shown in the figure. Ans. 7. The Examiner also finds that AAPA's signals EnF and En are provided by circuits that are external to the circuit shown in AAPA. *Id.* The Examiner

finds that AAPA as modified by Amirabadi includes a ninth transistor 134 that has a gate configured to receive a first bias signal (EnF or Amirabadi's GND) and a tenth transistor 126 that has a gate configured to receive a second bias signal (EN or Amirabadi's Vcc). *Id.* The Examiner finds that Vcc and GND of Amirabadi—as well as En and EnF of AAPA—are "generated externally" by circuits not shown in the figures. *Id.*

The Examiner finds that modified AAPA shows the "only a single transistor" limitations. *Id.; see* modified AAPA on page 10 *supra*.

Appellant argues that the amplifiers in AAPA are connected to transistors activated by enable signals, but not to a first or second bias signal. Appeal Br. 10. Appellant also argues that Amirabadi's Vcc and GND signals are not generated externally by a bias level generator and none of Amirabadi's transistors 124, 126, 132, or 134 is connected to a bias signal that is generated externally. *Id.* at 10–11; *see also* Reply Br. 6. Appellant contends that no explanation is provided as to why one would be motivated to combine AAPA with Amirabadi's teachings to provide a bias-type input buffer circuit. Appeal Br. 12.

Appellant's arguments are not persuasive.

Appellant does not respond to the Examiner's finding that disclosed signals Vcc and GND (or En and EnF) are provided by circuits not shown in the figures that are "externally generated." *See generally* Appeal Br., Reply Br. Rather, Appellant contends that Amirabadi "explicitly contradicts the Examiner's assertion" regarding Amirabadi, but argues only that Amirabadi discloses that the input buffer includes connections to GND through transistor 126 and to Vcc through transistor 134. Reply Br. 6. We do not perceive such disclosures by Amirabadi as "explicitly contradicting" the Examiner's position. We note, as well, the lack of argument regarding

AAPA's signals En and EnF as being provided by bias signals generated externally.

Regarding motivation, the Examiner indicates that the rejection does not propose combining AAPA with Amirabadi to provide a bias-type buffer circuit as Appellant contends. Ans. 8. The Examiner proposes using constant external bias voltages (Vcc and GND) for switchable external bias voltage (En and EnF) to bias AAPA's ninth and tenth transistors in order to provide a more stable buffer signal. *Id.* Appellant does not respond to the Examiner's statement on motivation. *See generally* Reply Br.

"As long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventors." *In re Beattie*, 974 F.2d 1309, 1312 (Fed. Cir. 1992); *see also In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). The motivation provided by the Examiner is sufficient when an allowance is made for "the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

Appellant argues that Amirabadi does not include only a single transistor connected between amplifier 101 and node 109, or between amplifier 102 and node 106. Appeal Br. 11. Appellant contends that transistors 126 and 124 must be included as a pair for amplifier 101 to operate properly, and transistors 132 and 134 must be included as a pair for amplifier 102 to operate properly. *Id.*

Appellant's arguments are unpersuasive of error by the Examiner because the Examiner relies on AAPA, not Amirabadi, to teach the "single transistor" limitations. *See* Ans. 7–8.

We determine for the reasons given above that the Examiner did not reversibly err in rejecting claim 11 as unpatentable over AAPA in view of Amirabadi. Accordingly, we also affirm the rejection of claims 12, 19, and 20, which depend from claim 11. 37 C.F.R. § 41.37(c)(1)(iv).

Claim 21

Independent claim 21 is very similar to claim 11. *Compare* Appeal Br. 19–20 (claims 11) *with id.* at 21–22 (claim 21). Claim 21 recites that a ninth and an eleventh transistor each has a gate configured to receive a first activation signal and a tenth and a twelfth transistor each has a gate configured to receive a second activation signal which is a complementary signal of the first activation signal. Appeal Br. 22 (Claims App'x).

The Examiner finds that AAPA discloses these limitations with En being a first activation signal, and EnF being a second activation signal that is a complementary signal of the first activation signal. Final Act. 6.

In addition to arguments made in relation to claim 11, Appellant argues that Amirabadi's Vcc signal is not a complementary signal of the GND signal. Appeal Br. 14. Appellant further argues that none of Amirabadi's transistors 124, 126, 132, or 134 is connected to an activation signal. *Id.*

We are not persuaded of reversible error by the Examiner in rejecting claim 21 at least because Appellant fails to address the Examiner's finding that AAPA discloses a first and second activation signal (En and EnF).

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–6, 8–12, 19–21	103	AAPA, Amirabadi	1–6, 8–12, 19–21	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED