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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEPHEN ALEXANDER,
PETER TREMAN, and
KENNETH JAMES McCAFFREY

Appeal 2019-004460
Application 14/845,882
Technology Center 3600

Before STEFAN STAICOVICI, MICHAEL L. HOELTER, and BRENT M. DOUGAL, *Administrative Patent Judges*.

HOELTER, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–12.[2] We have jurisdiction under 35 U.S.C. § 6(b). We REVERSE.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as "Ford Global Technologies, LLC." Appeal Br. 1.

[2] Claims 13–20 have previously been canceled, and claims 21–28 have been withdrawn.

CLAIMED SUBJECT MATTER

The disclosed subject matter "generally relates to vehicle computing systems, and more particularly, to a vehicle computing system communicating data to a remote server." Spec. ¶ 1. System claim 1 is the sole independent claim, is illustrative of the claims on appeal, and is reproduced below.

1. A vehicle system comprising:

a first communication processor (FCP) connected to a vehicle network;

a second communication processor (SCP) connected to the FCP; and

a vehicle processor configured to communicate with the FCP and SCP, and programmed to,

in response to received vehicle data via the vehicle network, communicate the vehicle data to a server via the FCP; and

in response to received infotainment data via the SCP, output the infotainment data to a display.

EVIDENCE

Name	Reference	Date
Tamura et al. ("Tamura")	US 2007/0022173 A1	Jan. 25, 2007
Nagara et al. ("Nagara")	US 2012/0330498 A1	Dec. 27, 2012

REJECTION

Claims 1–12 are rejected under 35 U.S.C. § 103 as unpatentable over Nagara and Tamura.

ANALYSIS

Claim 1 recites three processors, a "first communication processor," a "second communication processor," and a "vehicle processor."[3] The Examiner relies on Nagara for such disclosure, and specifically correlates "*one of modules 102, 104, 106*" to the first processor, and repeats this same correlation ("*another one of modules 102, 104, 106*") with respect to the second processor. Final Act. 5; *see also* Ans. 5 for more specific "mapping of Nagara to the claims." The Examiner relies on Tamura for other recited limitations. *See* Final Act. 6, *see also* Appeal Br. 7 ("[t]he rejection does not rely on the secondary reference to Tamura as disclosing or suggesting first and/or second communication processors").

Appellant's contention is that "the proposed combination of references taken as a whole fails to disclose or suggest a vehicle system having three (3) processors configured as recited in rejected Claim 1. As such, the rejection is improper and should be reversed." Appeal Br. 1–2. Appellant argues that the references fail "to disclose or suggest first and second communications processors" and that the Examiner "relies on an overly broad and unreasonable interpretation of the modules disclosed by Nagara et al., as being communication processors, which they clearly are not." Appeal Br. 2–3; *see also id*. at 4, 7.

[3] Appellant's Specification does not expressly define a processor, (i.e., a "microprocessor"), but employs such term in its ordinary and customary usage, and distinguishes the same from "memory devices (e.g., FLASH, random access memory (RAM) . . .) and software which co-act with one another to perform operation(s) disclosed herein." *See* Spec. ¶ 12; *see also* Spec. ¶ 17 (discussing "processor 3" which Appellant's Figure 1 illustrates as including a "CPU").

Nagara describes "at least one module **102**, **104**, **106** connected to a system (not shown) of a vehicle (not shown)." Nagara ¶ 17. Nagara also discusses "connectivity module **108**" (which the Examiner correlates to the third "vehicle processor" (*see* Ans. 5)) stating that this "connectivity module **108** can send requests for data to the at least one module **102**, **104**, **106**, and can receive requested data from the at least one module **102**, **104**, **106**." Nagara ¶ 18. Paragraph 19 of Nagara discloses a "data store **110**" that "permits read-only access of the at least one module **102**, **104**, **106**." Subsequent paragraphs of Nagara state, "the data store **110** includes a memory buffer **114** that temporarily holds data **116** from the at least one module **102**, **104**, **106**" and further that these modules "may have read/write access to the data store **110** for writing the data **116** to the buffer **114.**" Nagara ¶¶ 20, 21; *see also* Nagara Fig. 3.

"[T]he Examiner respectfully disagrees with Appellant that one having ordinary skill in the art would not consider modules 102, 104, 106 of Nagara as communications processors." Ans. 4. "Paragraph [0018] of Nagara teaches module 108 sends requests to 102, 104, 106 and receives data from them, thus making each module a transceiver." Ans. 5; *see also id*. at 6 ("modules 102, 104, 106 can send and receive vehicle data" (referencing Nagara ¶ 20)). However, even presuming each module is a transceiver, the Examiner does not explain how being a "transceiver" thereby renders each module a "processor," as this term is employed by Appellant in its ordinary and customary usage.

The Examiner further reasons "that it is impossible for these modules to communicate with one another without a 'brain' or processor which executes the instructions to send data." Ans. 5. The Examiner states, "one

having ordinary skill in the art would reasonably interpret these modules, in light of the disclosure of Nagara, as having processors in order to execute the instructions, otherwise they would not work as described." Ans. 5–6.

The Examiner's reasoning is not supported by a preponderance of the evidence for at least two reasons. First, Nagara itself discloses (i.e., "in light of the disclosure of Nagara") that it is "connectivity module **108**" that sends requests to and receives the requested data from modules 102, 104, 106. Nagara ¶ 18. Nagara teaches that this is accomplished via "data store **110**" that permits and/or controls access to the modules. *See* Nagara ¶¶ 19–23. In fact, Nagara clearly teaches, "[t]he data store **110** may further include a *processor* (not shown), in the case of the hardware implementation, for executing a program to monitor and approve/disapprove requests for the data." Nagara ¶ 21 (emphasis added). There is no comparable passage in Nagara regarding a processor with respect to modules 102, 104, and 106.

Second, is the Examiner's position that modules 102, 104, and 106 *inherently* have a "'brain' or processor which executes the instructions to send data." Ans. 5. Inherency, we have been instructed, requires more than agreement; inherency requires inevitability. *See Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003); *see also Par Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1196 (Fed. Cir. 2014). To be clear, an inherent disclosure requires that the prior-art reference "necessarily include the unstated limitation." *Atofina v. Great Lakes Chem. Corp.*, 441 F.3d 991, 1000 (Fed. Cir. 2006); *see also Cont'l Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991). "[P]robabilities or possibilities" are not enough to find that the prior art inherently discloses something not explicitly present. *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981).

As expressed above, Nagara is silent as to modules 102, 104, and 106 being processors. Instead, one skilled in the art, reading Nagara, would more reasonably understand these modules as data storage devices, in the manner of flash drives or other "memory devices," which Appellant's Specification distinguishes from a "microprocessor." *See* Spec. ¶ 12; *see also* Spec. Fig. 1. Thus, lacking both an express and an inherent disclosure in Nagara that each module 102, 104, and 106 is, or necessarily can be deemed to be, a "processor" (*see* Ans. 5, 6), we are not persuaded by the Examiner's reasoning.

The Examiner also proffers another mapping of Nagara to claim 1, but the Examiner still correlates each of modules 102, 104, and 106 to a "processor" (here, the "vehicle processor") in this "alternative hypothetical rejection." Ans. 6. For the reasons expressed above, the Examiner's alternative mapping contains the same discrepancy.

Accordingly, and based on the record presented, we reverse the Examiner's rejection of claims 1–12 as unpatentable over Nagara and Tamura.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s) /Basis	Affirmed	Reversed
1–12	103	Nagara, Tamura		1–12

REVERSED