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EXAMINER
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KARTHIKEYAN AVUDAIYAPAN

Appeal 2019-004381
Application 15/408,333
Technology Center 2100

Before KEVIN F. TURNER, JOYCE CRAIG, and SCOTT E. BAIN, *Administrative Patent Judges*.

BAIN, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–20, which constitute all pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Intel Corporation. Appeal Br. 2.

BACKGROUND

The Claimed Invention

The invention relates to cache memory access, and specifically, to minimizing delay in accessing a "last level cache" in a memory system. Spec. ¶¶ 1–4. Claims 1, 8, and 15 are independent. Claim 1 is illustrative of the invention and the subject matter in dispute, and is reproduced below:

> 1. A method for read request handling to minimize delay by a last level cache which interfaces with an external fabric, comprising:
>
> accessing a read request for a first read transaction;
>
> generating, external to the last level cache*, a phantom read transaction identifier for a second read transaction that is different than a read transaction identifier of said first read transaction*; and
>
> forwarding said second read transaction with said phantom read transaction identifier beyond a last level cache before detection of a hit or miss with respect to said first read transaction, and wherein said second read transaction is canceled *if* said first read transaction is a hit in said last level cache or does not access said last level cache.

Appeal Br. 13 (Claims App.) (emphases added).

References

The references relied upon by the Examiner are:

Name	Reference	Date
Hong	US 2003/0005226 A1	Jan. 2, 2003
Holland et al.	US 2014/0085320 A1	Mar. 27, 2014

The Rejection on Appeal

Claims 1–20 stand rejected under 35 U.S.C. § 103 as unpatentable over Hong and Holland. Final Act. 4–14.

DISCUSSION

We have reviewed the Examiner's rejection in light of Appellant's arguments presented in this appeal. Arguments that Appellant could have made but did not make in the Briefs are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(iv). For the reasons discussed below, Appellant has not persuaded us of error. To the extent consistent with the discussion below, we adopt as our own the findings and reasons set forth in the rejections and in the Examiner's Answer, and we provide the following for highlighting and emphasis.

Appellant argues the Examiner erred in finding the prior art teaches or suggests a "phantom read transaction identifier for a second read transaction that is different than a read transaction identifier of said first read transaction," as recited in claim 1. Appeal Br. 4–6. Specifically, Appellant argues Hong discloses only a "single read transaction," and the "generation and reconciling of two separate read transactions being sent to the cache and main memory [as Appellant alleges is recited in claim 1] is a problem that is not identified by either of the cited references." *Id.* at 6. We, however, are unpersuaded of error.

As the Examiner finds, Hong teaches "read requests from [a] processor are served by either the cache memory . . . or . . . main memory [], depending whether the requested data is present in the cache memory." Ans. 4; Hong Fig. 1, ¶ 5. In Hong, if the cache memory has the requested data (a

cache hit), the requested data are retrieved directly from the faster cache memory, and if the cache memory does not have the requested data (a cache miss), the requested data are fetched from the slower main memory. Ans. 5; Hong ¶ 5. Hong further teaches two corresponding read transactions originating from a read request, with the first read transaction directed toward the "cache memory" and the second read transaction directed toward the "main memory." Ans. 5–8; Hong ¶¶ 16–18. As the Examiner finds, Hong teaches the two read transactions to the (faster) cache memory and the (slower) main memory originate from a read request "simultaneously," which (as in Appellant's claim 1) reduces latency and time of obtaining the requested data. Ans. 6–7; Hong ¶¶ 5, 16–20.

In addition, the Examiner relies not on Hong alone for the disputed limitation, but on the combination of the foregoing teachings of Hong with Holland's teaching of "generating a read transaction/request identifier for each respective read transaction/request." Holland ¶ 39, claim 15; Final Act. 7–8; Ans. 9. Because "one cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references," *In re Keller*, 642 F.2d 413, 426 (CCPA 1981), we are not persuaded by Appellant's arguments regarding Hong individually. Further, Appellant's Specification acknowledges that it is known that any read transaction must have a read transaction "ID." Spec. ¶¶ 3–4; *see also* Ans. 9.

Appellant also argues that the references fail to teach or suggest "forwarding said second read transaction with said phantom read transaction identifier beyond a last level cache before detection of a hit or miss with respect to said first read transaction, and wherein said second read

transaction is canceled if said first read transaction is a hit in said last level cache or does not access said last level cache," as further recited in claim 1. Appeal Br. 7–8. Appellant argues that the Examiner erred in relying on the "same general interpretation" of the prior art as discussed above. *Id.* at 7. For the same reasons as discussed above, however, we are unpersuaded of error. Moreover, although not addressed by the Examiner, the "wherein" clause of the "forwarding" limitation is not entitled to patentable weight, because it is conditional (i.e., "canceled *if* said first read transaction is a hit . . ") (emphasis added). *See Ex parte Schulhauser*, Appeal 2013-007847, slip op. 6–10 (PTAB April 28, 2016) (precedential) (conditional "if" limitation in a method claim is afforded no patentable weight).

We also find that the Examiner has provided a sufficient rationale for combining the references (not substantively contested by Appellant):

> it would have been obvious for a person of ordinary skill[] [in] the art at the time of Applicant's invention to generate a read transaction/request identifier for each respective read transaction/request and including the read transaction/request identifier together with the associated read transaction/request to the memory, as demonstrated by Holland, and to incorporate it into the conventional system disclosed by Hong, *because Holland teaches doing so ensure[s] the matching of the returned data in response to the corresponding read transaction/ request*[.] [For example, Holland recites in claim 15] . . . 'identifying the data returned as being a response to the read request generated by the first requestor based at least in part on an identifier (ID) included in the read request.'

Final Act. 8; Ans. 12 (emphasis omitted); *see DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co*., 464 F.3d 1356, 1365 (Fed. Cir. 2006) (rationale to combine references also may be found within the

references themselves). Further, we note that no reply brief was filed, so there is no persuasive rebuttal of the Examiner's findings in the Answer.

Finally, Appellant argues the rejection of claim 2 separately, contending that the Examiner erred in finding the prior art teaches "the phantom read transaction identifier is converted to a pointer to a real read transaction identifier . . . ." Appeal Br. 8–9. Again, however, the disputed clause is part of a conditional limitation, i.e., this method step is only performed "*if* said first read transaction is a miss in said last level cache." Appeal Br. 13 (Claims App.) (quoting claim 2) (emphasis added). We, therefore, give the disputed clause no patentable weight. *See supra Ex parte Schulhauser*, Appeal 2013-007847, slip op. at 6–10. Accordingly, we are unpersuaded the Examiner erred.

The remaining claims are not argued separately. For the foregoing reasons, we are unpersuaded the Examiner erred, and we sustain the obviousness rejection of claims 1–20.

CONCLUSION

We affirm the Examiner's decision rejecting claims 1–20.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–20	103	Hong, Holland	1–20	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

AFFIRMED