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DICKE, BILLIG & CZAJA
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER
GUPTA, RAJ R

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ANTON MAUDER and PHILIPP SENG

Appeal 2019-004063
Application 14/620,772
Technology Center 2800

Before ROMULO H. DELMENDO, BEVERLY A. FRANKLIN, and MICHAEL P. COLAIANNI, *Administrative Patent Judges*.

COLAIANNI, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–5, 7 –13, 15, 16, and 25–30. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Infineon Technologies Austria AG. Appeal Br. 3.

Appellant's invention is directed to a semiconductor diode with an integrated resistor (Spec. ¶ 2; Claim 1).

Claim 1 is representative of the subject matter on appeal:

> 1. A semiconductor boot-strap diode with an integrated charge current resistor, comprising:
>
> a semiconductor body having a front surface and a back surface and including a cathode emitter zone defining the back surface;
> a cathode electrode;
> a cathode zone of a first conduction type;
> an anode zone of a second conduction type;
> a p-n junction between the cathode zone and the anode zone; and
> a single unitary resistance layer disposed between the cathode emitter zone and the cathode electrode, the unitary resistance layer in direct contact with the cathode electrode and having a surface disposed on and uninterruptedly extending over the entire back surface at the cathode emitter zone of the semiconductor body and forming no p-n junction therewith, and the resistance layer providing an integrated charge current resistor where the resistance layer is in resistive contact with the cathode emitter zone.

Appellant appeals the following rejections:

1. Claims 1–5, 7–13, 15, 16, and 25–30 are rejected under 35 U.S.C. § 112, first paragraph, as lacking written descriptive support.
2. Claims 1–5, 7, 8, 25, 26, 29, and 30 are rejected under 35 U.S.C. § 103(a) as unpatentable over Mauder (US 2005/0161746 A1, published July 28, 2005) in view of Tolonics (US 2006/0255376 A1, published Nov. 16, 2006).
3. Claims 9–13, 15, 16, 27, and 28 are rejected under 35 U.S.C. § 103(a) as unpatentable over Strzalkowski (US 2007/0081280 A1, published Apr. 12, 2007) in view of Mauder and Tolonics.

The Examiner objects to the Specification under 37 C.F.R. § 1.75(d)(1) because the Specification is silent regarding the formation of a p-n junction between the resistance layer and the semiconductor body or any lack thereof (Final Act. 2). Ordinarily, recourse for objections to the Specification are addressed by way of petition to the Director. *See*, Manual of Patent Examining Procedure (MPEP) § 1201. However, where, as here, the objection is determinative of the rejection, we may exercise our discretion to decide the merits of the objection as well. *See*, *In re Hengehold*, 440 F.2d 1395, 1403 (CCPA 1971) and *Ex parte Frye*, 94 USPQ2d 1072, 1078 (BPAI 2010). In the present case, our determination of the merits of the Specification objection is determinative of the propriety of the §112, first paragraph, written description rejection. We will address the merits of the Specification objection in our decision of the merits of the written description rejection.

FINDINGS OF FACT & ANALYSIS

Rejection (1): Written Description Rejection and Specification Objection

The Examiner finds that independent claim 1, 9, and 29 fail to comply with the written description requirement because the limitation "the unitary resistance layer . . . of the semiconductor body and forming no p-n junction therewith" lacks support in the written description (Final Act. 3). The Examiner finds that there is no discussion of forming the p-n junction or lack thereof in the original disclosure (Final Act. 3). The Examiner objects to the Specification as failing to provide proper antecedent basis for the claimed subject matter (Final Act. 2). The Examiner finds that the Specification is silent as to formation of a p-n junction between resistance layer and the

semiconductor body of any lack thereof as in claims 1, 9, and 29 (Final Act. 2).

Appellant argues that Figure 1 of the application shows that there is a diode structure (1) formed within the semiconductor layer 8, but no diode is shown for the connection between the resistive layer 7 and the semiconductor 8 (Appeal Br. 7–8). Appellant refers to paragraphs 22 to 24 of the Specification where Figure 1 is described (Appeal Br. 7). Appellant contends that "if a p-n junction was formed between resistance layer 12 and semiconductor body 8, a second diode symbol would have to be represented in the equivalent circuit diagram." (Appeal Br. 7). We agree.

The Examiner correctly finds that the claim limitation is a negative limitation (Ans. 4). The Examiner finds that Appellant's arguments are directed to a mere absence of a positive recitation, which cannot for the basis for the absence of a p-n junction between the resistive layer and the semiconductor (Ans. 4). The Examiner finds that circuit diagrams do not show all the features of the circuit, such as wire resistances, otherwise the diagram would be unreadable (Ans. 4).

Patent drawings may not be disregarded for items that they clearly show. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972). In this case, Appellant's figure 1 clearly shows that a diode 1 is formed over the semiconductor body 8, but no diode is formed between the resistive layer 7 and the semiconductor body 8. Resistive layer 7 includes the conventional resistor circuit diagram and diode 1 includes the typical diode symbol. The diode symbol 1 is connected to resistor 7 with no indication that another diode is formed or operates between resistive layer 7 and semiconductor body 8. *See* Figure 1. Although, the Examiner finds that the resistance layer

may be made of silicon which is suitable material to form a p-n junction, the Examiner does not explain why using silicon would necessarily produce a p-n junction between the resistance layer and the semiconductor material (Ans. 5). The preponderance of the evidence favors Appellant's argument of written descriptive support. We reverse the Examiner's § 112, first paragraph, rejection and the Examiner's objection to the Specification under 37 C.F.R. § 1.75(d)(1).

Rejections (2) and (3)

Claims 1 and 29

Claim 1 recites in relevant part "a single unitary resistance layer . . . in direct contact with cathode electrode and having a surface disposed on and uninterruptedly extending over the entire back surface at the cathode emitter zone and forming no p-n junction therewith."

Claim 29 recites in relevant part "a single unitary resistance layer disposed between the cathode emitter zone and the cathode electrode, the unitary resistance layer in direct contact with the cathode electrode and forming a non-pn junction interface with the cathode emitter zone. ..."

The Examiner finds that Mauder teaches a semiconductor boot-strap diode with an integrated charge current resistor (i.e., 8_1-8_4 in Figure 1) as recited in claims 1 and 29, except that Mauder does not teach a resistance layer is a single unitary resistance layer that forms no p-n junction with the semiconductor body (Final Act. 4–5). The Examiner finds that Tolonics teaches a resistance layer 200 as a single unitary resistance layer that forms no p-n junction with the semiconductor body so that the resistance value can be adjusted without changes in the layout and lithography masks being

necessary (Final Act. 5). The Examiner concludes that it would have been obvious to combine the semiconductor diode of Mauder with the resistance layer of Tolonics so that the resistance value can be adjusted without changes in the layout and lithography masks being necessary (Final Act. 5).

Appellant argues that neither Mauder nor Tolonics teaches a single unitary resistance layer disposed on and uninterruptedly extending over the entire cathode emitter zone, but forms no p-n junction therewith as required by claims 1 and 29 (Appeal Br. 9). Appellant further argues that modifying Mauder to use Tolonic's resistance layer would have changed Mauder's principle of operation (Appeal Br. 9). Appellant contends that Mauder uses p-n junctions J1, J2 and J3 to mitigate a space charge zone in the semiconductor device (Appeal Br. 10). Appellant argues that p-n junctions J2 and J3 are formed between p-type zones 8_1-8_4 and semiconductor layers 4 and 5 and are vital to Mauder's device (Appeal Br. 10). Appellant contends that a person of ordinary skill in the art would not have modified Mauder's diode to eliminate p-type regions 8_1 to 8_4 in favor of using Tolonic's resistor layer because doing so would have changed Mauder's principle of operation using the p-n junctions J2 and J3 and rendered the device unsatisfactory for its intended purpose (Appeal Br. 10–11). Appellant contends that the Examiner reversibly erred in finding that substituting Tolonic's resistor layer for Mauder's p-type structures 8_1-8_4 would have resulted in the same functionality (i.e., mitigating a space charge zone) (Appeal Br. 11; Reply Br. 8). Appellant argues that substituting Tolonic's resistance layer for Mauder's spaced apart p-type zones 8_1 to 8_4 changes the principle of operation of Mauder's diode by rendering it inoperable to preclude the build-

up of a space charge zone that could lead to the semiconductor's destruction (Reply Br. 8–9).

The Examiner responds that replacing the resistance layer appended to the diode of Mauder, which is more complex and more difficult to adjust and manufacture, with the simpler and easier to adjust and manufacture bulk resistor of Tolonics would not destroy the diode of Mauder (Ans. 7). The Examiner contends that Mauder is directed to a diode with an integrated resistor providing protection to the diode (Ans. 7). The Examiner finds that the proposed modification would only change the type of resistor, and not impact the overall principle of operation of the diode (Ans. 7). The Examiner finds that the principle of operation is directed to the diode, which would not have been modified by the proposed modification in the rejection (Ans. 7). The Examiner finds that no substantial reconstruction or redesign of the device would be necessary to modify Mauder with Tolonics' resistor (Ans. 7).

Although the Examiner finds that all that is involved is the simple substitution of Tolonics' resistor for Mauder's resistor, the Examiner fails to explain why making such a substitution would not have affected the p-n junctions J2 and J3 in Mauder. Mauder teaches:

> Thus, an *essential* aspect of the invention is, in the case of a high-voltage diode structure, improving the commutation strength by means of stabilizing dynamic avalanche at the cathode during switching. The semiconductor diode embodiments 1, 1' according to the invention make it possible to avoid destructive electric fields at an nn+ junction without the semiconductor diode having to have such a large central zone thickness that a dynamic "avalanche" at the pn junction of the semiconductor diode is ended before an electric field can form at the nn+ junction.

(emphasis added, ¶ 41).

The nn+ junction refers to junction J2, J3 as shown in Mauder's Figure 2 (¶¶ 37, 41). Mauder also teaches that the dimensions of the p-type area semiconductor zones 8_1 to 8_4 and their distances from one another and from the cathode modulate the flooding of the component with charge carriers (¶ 39). Mauder teaches that using the p-type areas 8_1-8_4 reduces forward voltage and switching losses in a targeted manner (¶ 39).

Based on Mauder's teachings, the particular p-type area 8_1-8_4 arrangement is required to achieve the mitigation of the space charge zone. The Examiner does not explain or provide evidence to substantiate that Tolonics' resistance layer would provide this necessary functionality for Mauder's diode. In other words, Mauder's teachings appear to indicate that the p-type area structures are necessary and modifying that structure to use Tolonics' resistance layer would appear to frustrate Mauder's purpose. Although Appellant argues to the contrary, the Examiner does not provide any objective evidence that Tolonics' resistance layer would function as the p-type area as in Mauder and mitigate the space charge zone (Ans. 7–8). On balance, we find that the preponderance of the evidence favors Appellant's argument of non-obviousness.

With regard to rejection (3), claim 9 is rejected under § 103 over Strzalkowski in view of Mauder and Tolonics (Final Act. 7). The Examiner relies on Strazalkowski to teach a bridge circuit (Final Act. 7). The Examiner relies on Mauder and Tolonics to teach the structure of the diode including the limitation, the "resistance layer is a single unitary resistance layer that forms no p-n junction with the semiconductor body" (Final Act. 8–9). In other words, the combination of Mauder and Tolonics is relied upon

for the same reason in rejecting claims 1 and 29 over that combination of art. As with rejections (1) and (2), we find that the preponderance of the evidence favors Appellant's argument of non-obviousness for the same reasons noted above.

We reverse the Examiner's § 103 rejection of claims 9–13, 15, 16, 27, and 28 over Strzalkowski in view of Mauder and Tolonics.

CONCLUSION

In summary:

Claims Rejected	Basis	Prior Art	Affirmed	Reversed
1–5, 7–13, 15, 16, 25–30	§ 112, ¶ 1			1–5, 7–13, 15, 16, 25–30
1–5, 7, 8, 25, 26, 29, 30	§ 103(a)	Mauder, Tolonics		1–5, 7, 8, 25, 26, 29, 30
9–13, 15, 16, 27, 28	§ 103(a)	Strzalkowski, Mauder, Tolonics		9–13, 15, 16, 27, 28
Overall Outcome				1–5, 7–13, 15, 16, 25–30

REVERSED