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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SHENG-HAO WANG, JIAN-DE JIANG,
CHIN-WEI TIEN, and CHIH-HUNG LIN

Appeal 2019-003998
Application 14/076,436
Technology Center 2100

Before ELENI MANTIS MERCADER, JASON J. CHUNG, and JOHN D. HAMANN, *Administrative Patent Judges*.

CHUNG, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals the Final Rejection of claims 1, 3–7, and 9–12.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

INVENTION

The invention relates to virtual time control. Spec. 1:10–14. Claim 1 is illustrative of the invention and is reproduced below:

> 1. A virtual time control apparatus, comprising:
> a system timer, having an original timer period;

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. According to Appellant, Institute for Information Industry is the real party in interest. Appeal Br. 1.

[2] According to the claim listing filed on September 30, 2017, claims 2 and 8 are cancelled.

> a real time clock, having an original tick period; and
>
> a processing unit, being electrically connected to the system timer and the real time clock and configured to execute a hypervisor and an operating system,
>
> *wherein the hypervisor is configured to generate a virtual timer period according to an adjustment ratio and the original timer period, generate a virtual tick period according to the adjustment ratio and the original tick period, generate a virtual real time clock, and generate a virtual real time according to the virtual real time clock and the virtual tick period*,
>
> wherein the virtual timer period is different from the original timer period and the virtual tick period is different from the original tick period,
>
> wherein the virtual real time is either accelerated when the adjustment ratio is greater than 1 or decelerated when the adjustment ratio is smaller than 1 with respect to the real time clock,
>
> wherein the hypervisor further provides the virtual real time to the operating system.

Appeal Br. 18 (Claims Appendix) (emphasis added).

REJECTIONS[3]

The Examiner rejects claims 1, 3, 4, 7, 9, and 12 under 35 U.S.C. § 103 as being unpatentable over the combination of Niesser (US 2013/0125118 A1; published May 16, 2013), Armstrong (US 2007/0028052 A1; published Feb. 1, 2007), and Yourst (*PTLsim:* A Cycle Accurate Full System x86-64 Microarchitectural Simulator). Final Act. 10–15.

The Examiner rejects claims 5 and 10 under 35 U.S.C. § 103 as being unpatentable over the combination of Niesser, Armstrong, Yourst, and Cui (US 2008/0240169 A1; published Oct. 2, 2008). Final Act. 15–16.

[3] The rejection of claims 1, 3–7, and 9–12 under 35 U.S.C. § 101 is withdrawn. Ans. 3.

The Examiner rejects claims 6 and 11 under 35 U.S.C. § 103 as being unpatentable over the combination of Niesser, Armstrong, Yourst, and Saeki (US 2002/0070783 A1; published June 13, 2002). Final Act. 16–17.

ANALYSIS

The Examiner finds Armstrong teaches a global system clock, an independent clock state delta value associated with each respective partition, and adjusting the global system clock by the partition's clock state delta to determine the clock value for a partition, which the Examiner maps to the limitation "wherein the hypervisor is configured to generate a virtual timer period according to an adjustment ratio and the original timer period, generate a virtual tick period according to the adjustment ratio and the original tick period" recited in claim 1 (and similarly recited in claims 7 and 12). Final Act. 12, 14, 15 (citing Armstrong ¶¶ 13, 26). The Examiner finds Yourst teaches a simulator running X times slower than the native CPU and both external interrupts and timer interrupts are theoretically generated X times slower than in the real world, which the Examiner maps to the limitation "generate a virtual real time clock, and generate a virtual real time according to the virtual real time clock and the virtual tick period" recited in claim 1 (and similarly recited in claims 7 and 12). Final Act. 13–15 (citing Yourst § 4.2). The Examiner explains Appellant fails to consider the combination of references. Ans. 2–7.

Appellant argues Armstrong is limited to adjusting only one type of original information, but fails to teach adjusting two types of original time information based on the same adjustment ratio. Appeal Br. 11; Reply Br. 4–5. Appellant argues Yourst merely teaches a simulator running X times slower than the native CPU and both external interrupts and timer interrupts

are theoretically generated X times slower than in the real world, but fails to teach any specific technical means, such as the specific relations between clock time, timers, and cycle rates and how these parameters mutually work. Appeal Br. 11–12; Reply Br. 3–4. We agree with Appellant.

As an initial matter, assuming Armstrong's clock state delta teaches the claimed "adjustment ratio," the cited portions of Armstrong is limited to adjusting only one type of original information, but fails to teach adjusting two types of original time information based on the same adjustment ratio as required by claim 1 (and similarly required by claims 7 and 12). Armstrong ¶¶ 13, 26 (cited at Final Act. 12, 14, 15).

Yourst does not remedy Armstrong's deficiencies. Yourst merely teaches a simulator running X times slower than the native CPU and both external interrupts and timer interrupts are theoretically generated X times slower than in the real world, but fails to teach adjusting two types of original time information based on the same adjustment ratio. Yourst § 4.2 (cited at Final Act. 13–15). In addition, neither the cited portions of Yourst nor the Examiner explain sufficiently how Yourst teaches the specific relationship between clock time, timers, and cycle rates and how these parameters mutually work. Yourst § 4.2 (cited at Final Act. 13–15).

Accordingly, we do not sustain the Examiner's rejections of: (1) independent claims 1, 7, and 12; and (2) dependent claims 3–6 and 9–11 under 35 U.S.C. § 103.

CONCLUSION

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 3, 4, 7, 9, 12	103	Niesser, Armstrong, Yourst		1, 3, 4, 7, 9, 12
5, 10	103	Niesser, Armstrong, Yourst, Cui		5, 10
6, 11	103	Niesser, Armstrong, Yourst, Saeki		6, 11
Overall Outcome				1, 3–7, 9–12

REVERSED