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Patterson + Sheridan, LLP - VMware
24 Greenway Plaza
Suite 1600
Houston, TX 77046

EXAMINER	
ZOUBAIR, NOURA	

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte WEI XU, ALOK NEMCHAND KATARIA,
RAKESH AGARWAL, and MARTIM CARBONE

Appeal 2019-003989
Application No. 14/550,881[1]
Technology Center 2400

Before MARC S. HOFF, ELENI MANTIS MERCADER, and
BETH Z. SHAW, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 1–3, 6–9, 12–15, and 18.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm in part.

Appellants' invention is an interrupt security module that handles interrupts without exposing a secret value of a register to virtual interrupt

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[1] Appellants state that the real party in interest is VMWare, Inc. Appeal Br. 3.

[2] Claims 4, 5, 10, 11, 16, and 17 have been cancelled.

handling code that executes at a lower privilege level. Upon receipt of such an interrupt, the interrupt security module overwrites the secret value of the register with an unrelated constant, generates a virtual interrupt, and forwards the virtual interrupt to the virtual interrupt handling code. Abstract.

Claim 1 is reproduced below:

> 1. A method of securing secret values stored in registers in a computer system operable in a plurality of privilege levels, wherein the method executes at a first privilege level and comprises:
>
> intercepting a first interrupt or exception that is targeted to an operating system executing instructions at a second privilege level, the instructions including a move instruction that sets a register to a secret value by moving an immediate value in the move instruction into the register, a compare instruction that determines whether or not the register contains the secret value by comparing a pre-determined erasure constant with contents of the register containing the secret value, and instructions that rely on the register containing the secret value for correct processing of the instructions,
>
> wherein the second privilege level is lower than the first privilege level and the first interrupt or exception is triggered during execution of the instructions that are executing at the second privilege level;
>
> in response to the intercepting, overwriting the secret value stored in the register with a pre-determined erasure constant; and
>
> then forwarding the first interrupt or exception to the operating system for handling of the first interrupt or exception by the operating system, wherein the operating system interprets the pre-determined erasure constant stored in the register as a trigger to re-execute the instructions.

The prior art relied upon by the Examiner as evidence is:

Name	Reference	Date
Orion et al. "Orion"	US 2009/0177830 A1	July 9, 2009
Henry et al. "Henry"	US 2014/0195821 A1	July 10, 2014
Jebson et al. "Jebson"	US 2014/0351472 A1	Nov. 27, 2014

Claims 1, 2, 7, and 13 stand rejected under 35 U.S.C. § 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellants regards as its invention. Ans. 3.[3]

Claims 1–3, 6–9, 12–15, and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Jebson, Henry, and Orion. Final Act. 3.

Throughout this decision, we make reference to the Appeal Brief ("Appeal Br.," filed November 28, 2018), the Reply Brief ("Reply Br.," filed April 26, 2019), and the Examiner's Answer ("Ans.," mailed March 5, 2019) for their respective details.

ISSUES

1. Does the combination of Jebson, Henry, and Orion teach or suggest an operating system executing a move instruction that sets a register to a secret value by moving an immediate value in the move instruction into the register?

2. Does the combination of Jebson, Henry, and Orion teach or suggest an operating system executing a compare instruction that determines whether or not the register contains the secret value by comparing a pre-

[3] The Examiner states that "amendments that would obviate these rejections have been agreed upon," but in the Advisory Action mailed October 1, 2018, Appellants' proposed amendments were not entered.

determined erasure constant with contents of the register containing the secret value?

3. Does the combination of Jebson, Henry, and Orion teach or suggest that the operating system interprets the pre-determined erasure constant stored in the register as a trigger to re-execute the instructions?

ANALYSIS

35 U.S.C. § 103 Rejection

Representative claim 1 recites in pertinent part a method of storing secret values stored in registers in a computer system, including intercepting a first interrupt or exception targeted to an operating system executing instructions at a second privilege level, those instructions including a move instruction that sets a register to a secret value by moving an immediate value in the move instruction into the register, and including a compare instruction that determines whether or not the register contains the secret value by comparing a pre-determined erasure constant with contents of the register containing the secret value. Independent claims 7 and 13 also recite these instructions.

The Examiner finds that Henry teaches the claimed move instruction. Ans. 14. The Examiner characterizes Henry as teaching an embodiment where immediate data "is moved to a secure memory area or register." *Id.*; Henry ¶ 73.

We find that the Examiner erred. The claim requires "a move instruction that sets a *register* to a secret value by moving an immediate value . . . into the *register*" (emphasis added). Appellants argue, and we agree, that the claim does not recite moving immediate data to a secure

memory area, and that a secure memory area is not equivalent to registers used by instructions of a processor. Reply Br. 4.

With respect to the recited compare instruction, the Examiner finds that Orion teaches register 2600 as containing a secret value in line-1 when the flag portion has value S. Ans. 15; Orion Fig. 55, ¶¶ 521–530.

We find that the Examiner erred in finding that Orion teaches the claimed instruction. Appellants argue, and we agree, that Orion Figure 55 concerns a cache in a memory management unit (MMU), rather than one or more registers. Reply Br. 5. The flag portion S in Orion is a readable value stored in a cache, not a secret value stored in a register. *Id.*

Representative claim 1 further recites that the operating system "interprets the pre-determined erasure constant stored in the register as a trigger to re-execute the instructions." Independent claims 7 and 13 also contain this limitation.

In the Final Rejection, the Examiner cited to Orion as teaching this limitation. Final Act. 9. The Examiner found that Orion teaches "a control parameter indicative of whether processing of a function should be resumed from the point where it was interrupted or whether it should be repeated following the interrupt." Orion ¶ 26.

Appellants argue, and we agree, that Orion's restarting of a function does not correspond to re-executing instructions that rely on the register containing the secret value for correct processing of the instructions, as is claimed. Appeal Br. 14. We further agree with Appellants that the control parameter of Orion is a register accessible by the processor, rather than the claimed pre-determined erasure constant. *Id.*

The Examiner, in the Answer, finds Appellants' argument unpersuasive because the Examiner alleges that the rejection relied on

Henry, rather than Orion, to teach this limitation. Ans. 17. In our review of the Final Rejection, however, the Examiner relies on Orion as teaching this limitation, and we have not located in the record any reliance on teachings in Henry for this limitation. Final Act. 9–10.

On this record, we therefore find that the combination of Jebson, Henry, and Orion fails to teach all the elements of the claimed invention. We do not sustain the Examiner's § 103 rejection.

35 U.S.C. § 112(b) rejection

The Examiner maintains the § 112 rejection of claims 1, 2, 7, and 13. Ans. 3. While "amendments that would obviate these rejections have been agreed upon," the Advisory Action mailed October 1, 2018, responding to such amendments, indicated that the proposed amendments were not entered.

Appellants have not contested the § 112 rejection in the Appeal Brief or in the Reply Brief. Therefore, we affirm *pro forma* the Examiner's § 112 rejection of claims 1, 2, 7, and 13.

CONCLUSIONS

1. The combination of Jebson, Henry, and Orion does not teach or suggest an operating system executing a move instruction that sets a register to a secret value by moving an immediate value in the move instruction into the register.

2. The combination of Jebson, Henry, and Orion does not teach or suggest an operating system executing a compare instruction that determines whether or not the register contains the secret value by comparing a pre-determined erasure constant with contents of the register containing the secret value.

3. The combination of Jebson, Henry, and Orion does not teach or suggest that the operating system interprets the pre-determined erasure constant stored in the register as a trigger to re-execute the instructions.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/ Basis	Affirmed	Reversed
1, 2, 7, 13	112(b)	Indefiniteness	1, 2, 7, 13	
1–3, 6–9, 12–15, 18	103	Jebson, Henry, Orion		1–3, 6–9, 12–15, 18
Overall Outcome			1, 2, 7, 13	3, 6, 8, 9, 12, 14, 15, 18

The Examiner's decision to reject claims 3, 6, 8, 9, 12, 14, 15, and 18 is reversed. The Examiner's decision to reject claims 1, 2, 7, and 13 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED IN PART