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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/763,003	04/19/2010	Ryan James Goss	STL16191	4656

73462 7590 10/14/2020

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EXAMINER	
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ART UNIT	PAPER NUMBER
2136	

NOTIFICATION DATE	DELIVERY MODE
10/14/2020	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte RYAN JAMES GOSS, KEVIN GOMEZ,
MARK ALLEN GAERTNER, and BRUCE DOUGLAS BUCH

Appeal 2019-003976
Application 12/763,003
Technology Center 2100

Before ROBERT E. NAPPI, JEAN R. HOMERE, and
JAMES R. HUGHES, *Administrative Patent Judges.*

HOMERE, *Administrative Patent Judge.*

DECISION ON APPEAL

I. STATEMENT OF THE CASE[1]

Pursuant to 35 U.S.C. § 134(a), Appellant appeals from the Examiner's decision rejecting claims 1–4, 7–16, 18, 19, and 21, all of the claims pending.[2] Claims App. Claims 5, 6, 17, and 20 have been canceled. *Id.* We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing was held

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[1] We refer to the Specification filed Apr. 19, 2010 ("Spec."); the Final Office Action, mailed June 4, 2018 ("Final Act."); the Appeal Brief, filed Dec. 6, 2018 ("Appeal Br."); the Examiner's Answer, mailed Feb. 26, 2019 ("Ans."); and the Reply Brief, filed April 26, 2019 ("Reply Br.").

[2] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Seagate Technology LLC as the real party-in-interest. Appeal Br. 1.

in this appeal on September 23, 2020. A transcript of the oral hearing will be entered into the record in due course.

We affirm, and designate our affirmance as a new ground of rejection.

II. CLAIMED SUBJECT MATTER

According to Appellant, the claimed subject matter relates to a method and system for updating stored user data in memory (118) in response to receiving access commands from computer host (102). Spec., 6:8–14.

Figures 1 and 6, reproduced and discussed below, are useful for understanding the claimed subject matter:

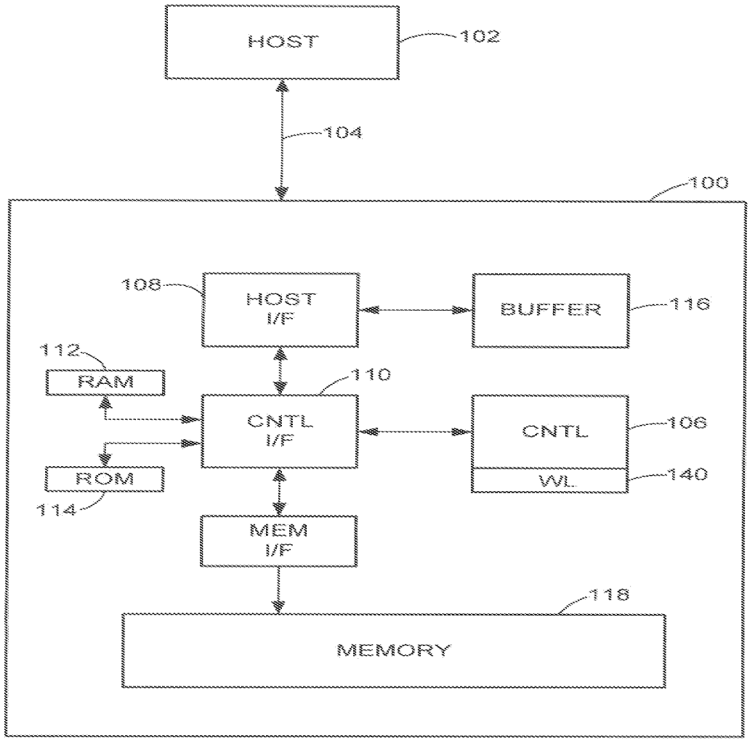

FIG. 1

Figure 1 above illustrates host (102) sending commands to storage device (100) via interface (104) to update user data in memory (118). *Id.* at 3:21–25.

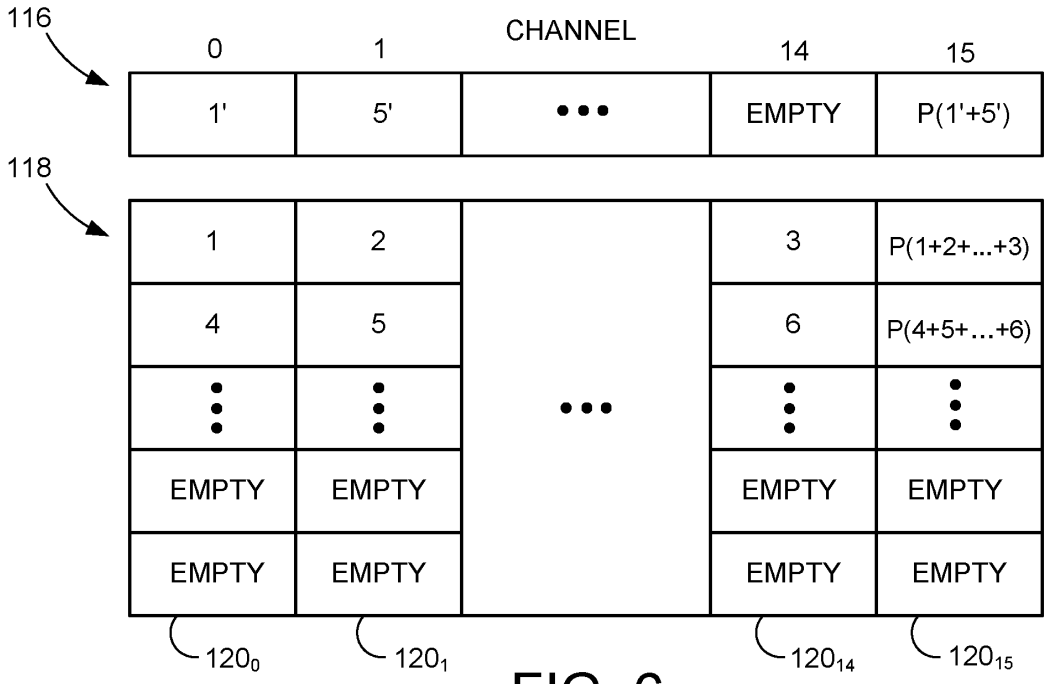

FIG. 6

Figure 6 above illustrates memory (118) having a plurality of channels (ch. 0–15) for storing full stripes of user data (ch. 0–14) along with associated parity data (ch. 15) accessible via buffer (116) having indices aligned with the channels for temporarily storing updated data for users 1' and 5' in channels 0 and 1 respectively. *Id.* at 2:15–17, 7:7–13.

In particular, responsive to the host access commands to update first and second user data (e.g., users 1 and 5) stored in the full stripes of memory (118), controller (106) executes memory control logic (140) that computes new parity data (P (1' +5')) for a partial stripe stored in buffer (116) including the updated first and second user data without using old user data and old parity data stored in memory (118). *Id.* at 7:7–13.

Claims 1, 13, and 21 are independent. Claim 1, reproduced below with disputed limitations emphasized, is illustrative:

> 1. A data storage apparatus configured to store data and in communication with a computer host to receive host access commands to update stored data, the data storage apparatus comprising:
>
> a memory having a predetermined plurality of channels storing full stripes of data, each full stripe of data storing user data from the computer host in each of a predetermined subset of the channels and storing parity data in each of the rest of the channels that is computed for the user data stored in the respective full stripe;
>
> a buffer having indices aligned with the channels in the memory and temporarily storing updated user data from the computer; and
>
> a processor-based controller executing memory control logic that, responsive to the host access commands to *update first user data stored in one of the full stripes in the memory and to update second user data stored in another one of the full stripes in the memory, computes new parity data for a partial stripe stored in the buffer that includes the updated first and second user data without using any old user data and without using any old parity data stored in the memory*.

Appeal Br. 11 (Claims App.).

III. REFERENCES

The Examiner relies upon the following references.[3]

Name	Reference	Date
Neufeld	US 5,333,305	July 26, 1994
Santeler	US 2002/0194530 A1	Dec. 19, 2002

[3] All reference citations are to the first named inventor only.

IV. REJECTION

The Examiner rejects claims 1–4, 7–16, 18, 19, and 21 under 35 U.S.C. § 103 as being unpatentable over the combined teachings of Santeler and Neufeld. Final Act. 2–5.

V. ANALYSIS

We consider Appellant's arguments in the order they are presented in the Appeal Brief, pages 5–10 and the Reply Brief, pages 2–10.[4]

Appellant argues that the Examiner erred in finding that the combination of Santeler and Neufeld teaches or suggests updating user data stored in full stripes contained in memory by computing new parity data for a partial stripe of the updated data stored in a buffer without using old data from memory, as recited in independent claims 1, 13, and 21. Appeal Br. 5. In particular, Appellant argues that Neufeld does not cure the admitted deficiencies of Santeler because Neufeld updates data already stored in memory by writing updated data back to the same stripe in which old data was stored. *Id.* at 7 (citing Neufeld 2:50–51, 3:35–44). According to Appellant, Neufeld expressly requires reading old data stored in memory when writing a partial stripe of updated data, whereas the disputed limitation requires using new data in a partial stripe as opposed to using old data in a full stripe to compute new parity data. *Id.* Further, Appellant argues that Neufeld teaches determining whether the stripe contains unused storage space wherein old data resides, whereas the disputed limitation requires old

[4] We have considered in this Decision only those arguments Appellant actually raised in the Briefs. Arguments not made are waived. *See* 37 C.F.R. § 41.37(c)(1)(iv) (2014).

data residing in a stull stripe in the memory contains no unused space. *Id.* at 8 (citing Neufeld Fig. 5). In particular, Appellant argues that Neufeld teaches reading old data from memory prior to computing the new parity data, which is subsequently written in the partial stripe of new data. *Id.* at 8–9. According to Appellant, Neufeld at best teaches writing dummy data to fill unused space after new parity data has already been computed from old data for the partial stripe of updated data. *Id.* at 9–10. Consequently, Appellant argues that the combination of Santeler and Neufeld would not have reasonably taught or suggested the disputed limitations of claims 1, 13, and 21. *Id.* at 10.

Appellant's arguments are not persuasive of reversible Examiner error because they are tantamount to attacks against the references' teachings individually, and not as the combination proposed by the Examiner. One cannot show non-obviousness by attacking the references individually where the rejections are based on combined teachings of the references. *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *see also In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

As a preliminary matter, we note the disputed claim limitation requires computing new parity data for a partial stripe using updated user data in a buffer (as opposed to user old data from memory) to thereby update old user data in full stripes contained in memory. The Examiner relies upon Santeler for its teaching of a memory module having stored in full stripes user data and parity data. Final Act. 2–3 (citing Santeler ¶¶ 29–31, 36, 37). The Examiner further relies upon Santeler for its teaching of a buffer logic computing new parity data in partial stripes, and writing new data in full stripes without retrieving old data from memory. *Id.* at 3 (citing Santeler

¶ 51). Additionally, the Examiner relies upon Neufeld for its teaching of performing a partial write operation without reading old data during which unused space will not be filled. *Id.* (citing Neufeld 3:45–52); Ans. 3 (citing Neufeld 10:3–15).

Although the Examiner also finds that Santeler teaches calculating partial strip parity using old data, we determine that this teaching to be cumulative. *Id.*[5] We find nonetheless that the combination of the cited teachings of Santeler and Neufeld is no more than a simple arrangement of old elements with each performing the same function it had been known to perform, yielding no more than what one would expect from such an arrangement. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Therefore, the ordinarily skilled artisan, being "a person of ordinary creativity, not an automaton," would have been able to fit the teachings of the cited references together like pieces of a puzzle to predictably achieve a buffer logic performing a partial stripe operation and computing new parity data using the updated data stored in a buffer without using old data from full stripes contained in memory and thereby updating user data in memory. Because Appellant has solely addressed Neufeld's teachings without addressing the merits of Santeler's teachings, Appellant has not demonstrated that the Examiner's proffered combination would have been "uniquely challenging or difficult for one of ordinary skill in the art." Therefore, we agree with the Examiner that the proposed modification would have been within the capabilities of the ordinarily skilled artisan. *See*

[5] Because we have modified the Examiner's proposed combination of Santeler and Neufeld, we designate our affirmance of the Examiner rejection as a new ground of rejection.

Leapfrog Enters., Inc. v. Fisher-Price, Inc., 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418). Consequently, we are satisfied that, on this record, that the combination of Santeler and Neufeld would have taught or at least suggested updating user data stored in full stripes contained in memory by computing new parity data for a partial stripe of the updated data stored in a buffer without using old data from memory. Ans. 4–6. Accordingly, we are not persuaded of error in the Examiner's rejection of claims 1, 13, and 21 over the combined teachings of Santeler and Neufeld.

Regarding the rejection of claims 2–4, 7–12, 14–16, 18, and 19, Appellant has not presented separate patentability arguments or has reiterated substantially the same arguments as those previously discussed for the patentability of claims 1, 13, and 21. As such, claims 2–4, 7–12, 14–16, 18, and 19 fall therewith. *See* 37 C.F.R. § 41.37(c)(1)(iv).

VI. CONCLUSION

We affirm the Examiner's rejections of claims 1–4, 7–16, 18, 19, and 21. 37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b)) as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. . . .

> (2) *Request rehearing*. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record. . . .

VII. DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/ Basis	Affirmed	Reversed	New Ground
1–4, 7–16, 18, 19, 21	103	Santeler, Neufeld	1–4, 7–16, 18, 19, 21		1–4, 7–16, 18, 19, 21

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED
37 C.F.R. § 41.50(b)