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W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

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PARK, ILWOO

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte LALAN JEE MISHRA and RICHARD DOMINIC WIETFELDT

Appeal 2019-003387
Application 14/994,242
Technology Center 2100

BEFORE ERIC B. CHEN, MICHAEL J. STRAUSS, and GREGG I. ANDERSON, *Administrative Patent Judges.*

ANDERSON, *Administrative Patent Judge.*

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–19. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

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[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as QUALCOMM Incorporated. Appeal Br. 2.

CLAIMED SUBJECT MATTER

The claims are directed to Signaling Protocols for Radio Frequency Front-End Control Interface (RFFE) Buses. Spec.,[2] Title. The "RFFE protocol is modified to provide addresses that are shorter than the normal four bits allocated by the RFFE protocol." *Id.* ¶ 18. This modification results in improved bus turnaround time, which reduces overall latency. *Id.* A "bus management portion may be sent using a single data rate (SDR), and a payload portion may be sent using a double data rate (DDR)," again reducing bus turnaround time and latency. *Id.*

Independent claims 1 and 11, reproduced below, are illustrative of the claimed subject matter:

> 1. A method of constructing an address field for a frame on a radio frequency front-end control interface (RFFE) bus, the method comprising:
>
> ascertaining a total number of addresses for devices associated with an RFFE bus;
>
> calculating a number of bits required to provide the total number of addresses; and
>
> setting a bit-field address-field length for a frame at a minimum number of bits based on the calculating.
>
> 11. A method of transmitting a frame on a radio frequency front-end control interface (RFFE) bus, the method comprising:

[2] We use "Spec." to refer to the Specification filed January 13, 2016, "Final Act." to refer to the Final Action mailed April 23, 2018, "Appeal Br." to refer to the Appeal Brief filed September 26, 2018, "Ans." to refer to the Examiner's Answer filed February 8, 2019, and "Reply Br." to refer to the Reply Brief filed March 28, 2019.

transmitting a first portion of a frame over an RFFE bus using a single data rate (SDR) technique; and

transmitting a second portion of the frame over the RFFE bus using a double data rate (DDR) technique.

REFERENCES

The prior art relied upon by the Examiner is:

Name	Reference	Date
Onufryk	US 2006/0282603 A1	Dec. 14, 2006
Fan	US 2010/0124176 A1	May 20, 2010
Kessler	US 2016/0041941 A1	Feb. 11, 2016

REJECTIONS

Claims 11, 12, 14, 15, and 19 are rejected under 35 U.S.C. § 102(a)(2) as being anticipated by Kessler. Final Act. 6–11.

Claims 1–8, 13, and 16–18 are rejected under 35 U.S.C. § 103 as being obvious over Onufryk and Kessler. *Id.* at 11–31.

Claims 9 and 10 are rejected under 35 U.S.C. § 103 as being obvious over Onufryk, Kessler, and Fan. *Id.* at 31–33.

OPINION

Issue 1: As recited in claim 11, are "single data rate (SDR) technique" and "double data rate (DDR) technique" disclosed in Kessler?

The Examiner's anticipation rejection of claim 11 relies on Kessler to disclose Issue 1. Final Act. 6–8 (citing Kessler ¶¶ 42, 138). According to the Examiner, the claimed single data rate (SDR) is disclosed in paragraph 42, which explains how "the master node 102 may transmit a synchronization control frame every 1024 bits (representing a superframe) at a frequency of 48 kHz." *Id.* at 7 (citing Kessler ¶ 42). The Examiner cites Kessler's paragraph 138 for the double data rate (DDR), citing Kessler's

disclosure that "[i]nstead of using a single data slot per single superframe (which is 48 kHz data rate) for the slave node 104, the data rate on the bus for transmitting to the slave 104 is doubled by having two data slots per superframe." *Id.* at 7–8 (citing Kessler ¶ 138 ("two data slots to double the superframe rate")).

Appellant argues "single data rate technique" and "double data rate technique" are "terms of art in the industry and accordingly have meanings to someone of ordinary skill in the art which constrains the interpretation afforded these terms." Appeal Br. 7–8 (citing Gelman[3] (US 2013/0082738 Al, Apr. 4, 2013); Spec. ¶ 34). Paragraph 34 of the Specification explains the following:

> Specifically, in an exemplary aspect, the bus management portion 120 of the frame is sent using an SDR as is set forth in the RFFE protocol. However, the payload portion of the frame is sent using a DDR. By sending data on both the rising and falling edge of the data, the speed of delivery of the payload portion is effectively doubled.

Id. (quoting Spec. ¶ 34).

Appellant contends that Kessler does not disclose "SDR" nor "DDR" but "merely a frequency." Appeal Br. 8–9. Thus, Appellant contends that when the proper definition of these terms is used, "it is clear that Kessler does not teach either SDR or DDR techniques." *Id.* at 7. As such, "Kessler

[3] Gelman is first cited in the Appeal Brief and is not of record. *See* 37 C.F.R. § 41.33(d)(1) (". . . Evidence filed after the date of filing an appeal pursuant to §41.31(a)(1) through (a)(3) and *prior to the date of filing a brief . . . may be admitted* if the examiner determines that the affidavit or other Evidence *overcomes all rejections under appeal* and that a showing of good and sufficient reasons why the affidavit or other Evidence is necessary and was not earlier presented has been made.") (emphasis added).

cannot anticipate claim 11." *Id.*

In the Answer, the Examiner contends "[a]lthough the claims are interpreted in light of the specification, limitations from the specification are not read into the claims." Ans. 29–30 (citing *In re Van Geuns*, 988 F.2d 1181 (Fed. Cir. 1993)).[4] The Examiner again cites paragraph 138 of Kessler for the recited "double data rate." *Id.* at 30.

We are not persuaded that SDR and DDR are terms of art. Appellant asserts paragraph 34 of the Specification supports its argument to the contrary. Appeal Br. 7–8 (citing Spec. ¶ 34). There is insufficient evidence of record that SDR and DDR are actually a part of the RFFE protocol, as paragraph 34 asserts,[5] neither is there any definition of the terms or other description that distinguishes the argued terms over the teachings of Kessler. Absent a specific meaning to a person of ordinary skill in the art, the broadest reasonable interpretation of SDR is a single data rate and of DDR is a double data rate.

We agree with the Examiner that Kessler discloses a single data rate at a frequency of 48 kHz. Final Act. 7 (citing Kessler ¶ 42); Ans. 4. The Examiner cites Kessler's paragraph 138 for the double data rate, "[i]nstead of using a single data slot per single superframe (which is 48 kHz data rate) for the slave node 104, the data rate on the bus for transmitting to the slave

[4] For the first time, the Examiner cites "UART (universal asynchronous receiver transmitter) has a single data rate and a double data rate . . . ." *Id.* at 30; *see also* Reply Br. 2 (UART is "new" and another disclosure of frequency).

[5] We have reviewed MIPI Alliance, Inc. *MIPI Alliance Specification for RF Front-End Control Interface*, Version 1.10 (July 2011). Although not of record, the terms "SDR" and "DDR" do not appear in the document. *See also* fn. 3 (Gelman is also not of record).

104 is doubled by having two data slots per superframe." *Id.* at 7–8 (citing Kessler ¶ 138 ("two data slots to double the superframe rate")); Ans. 4–5. Because the argued limitations are disclosed in Kessler, the rejection is sustained.

Appellant does not separately argue dependent claims 12, 14, and 15. *See generally* Appeal Br. 7–9. Accordingly, we sustain the rejection to these claims. Independent claim 19 is found unpatentable by the Examiner based on the all but the same disclosures of Kessler cited in connection with claim 11. *See* Final Act 9–11 (citing Kessler ¶¶ 42, 138). Appellant relies on its arguments for claim 11. Appeal Br. 9. For the same reasons discussed above in connection with claim 11, we sustain the rejection of claim 19.

Issue 2: As recited in claim 1, does Onufryk teach "setting [the] bit-field address-field length for a frame . . . based on the calculating?"

The Examiner's obviousness rejection of claim 1 relies on Onufryk to teach Issue 2. Final Act. 15–17 (citing Onufryk ¶¶ 13, 47). The stated limitation of allowed bits on a virtual bus is 2^4, resulting in no more than 16 devices to reside on each special bus. *Id.* at 15 (citing Onufryk ¶ 13). Each ID Tag or address can include an 8-bit "Bus" for a maximum of maximum of 32 devices. *Id.* at 16 (citing Onufryk ¶ 10). Stated another way, the bits of each bus are associated with a maximum number of addressed devices.

Appellant explains that in Onufryk, if the

> "[a]t least one of the plural virtual buses is . . . limited to having no more than 16 devices" but only four devices are coupled to the "virtual bus," there is no teaching or suggestion that the "number of bits . . . in the 'Device' identifying field" is actually set to two (i.e., the minimum number of bits based on the calculating).

Appeal Br. 10. Appellant argues "[t]he claim calculates 'based on how many devices are actually on the bus.'" *Id.* at 11. Furthermore, Appellant contends the setting of bits in Onufryk is not "'based on the calculating,' and thus, Onufryk does not teach or suggest the claim element." *Id.*

In the Answer, the Examiner all but repeats the prior findings based on paragraphs 10 and 47 of Onufryk. Ans. 12–13 (citing Onufryk ¶¶ 13, 47). In addition, the Examiner argues Appellant does not "specifically point[] out how the language of the claims patentably distinguishes them from the references." *Id.* at 30–33. The Examiner argues "based on the calculation" is taught through Onufryk's teaching that "**no more than 16 devices to reside on each special bus reduces the number of bits needed in the 'Device' identifying field of a corresponding ID Tag to 4 or less,**" setting a number of bits required. *Id.* at 31–32.

Appellant argues in its Reply,

> as recited in claim 1, there is a step of "ascertaining a total number of addresses" (e.g., 4) and from this "calculating a number of bits required to provide the total number of addresses" (e.g., 2). The "total number of bits" cannot be calculated unless there is an ascertainment of the "total number of addresses." In contrast, . . . Onufryk sets the "3-bit wide data field" first and then notes that it supports "up to eight domestic devices," regardless of how many devices are actually present.

Reply Br. 2.

We agree with Appellant that the claim limitation recites a calculation "based on how many devices are actually on the bus." *See* Appeal Br. 9–11. We are persuaded that Onufryk does not teach "setting [the] bit-field address-field length for a frame . . . based on the calculating." Rather, the bit-field is set by the size of the virtual bus. Onufryk ¶ 13 ("At least one of the plural virtual buses is designated by the switch's software or by other

means as a special bus that is limited to having no more than 16 devices (=2^4 devices) on it."). Thus the bit-field size is set and not calculated. Because the limitation are not taught by Onufryk, the rejection is not sustained.

Because claim 1 has not been shown to be unpatentable, dependent claims 2–8, 13, and 16–17 have not been shown to be unpatentable and we do not sustain the rejection to those claims. Independent claim 18 includes similar limitations (i.e., "set a bit-field address-field length for a frame at a minimum number of bits based on the calculating") to those argued in connection with independent claim 1 (i.e., "setting a bit-field address-field length for a frame at a minimum number of bits based on the calculating"). Claim 18 is found unpatentable by the Examiner based on the all but the same disclosures of Kessler cited in connection with claim 11. *See* Final Act 28–30 (citing Onufryk ¶¶ 13, 47). For the same reasons discussed above in connection with claim 1, we do not sustain the rejection of claim 18.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
11, 12, 14, 15, 19	102(a)(2)	Kessler	11, 12, 14, 15, 19	
1–8, 13, 16–18	103	Onufryk, Kessler		1–8, 13, 16–18
9, 10	103	Onufryk, Kessler, Fan		9,10
Overall Outcome			11, 12, 14, 15, 19	1–19

AFFIRMED-IN-PART