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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CHUN WANG

Appeal 2019-003245
Application 15/412,294
Technology Center 2600

Before LARRY J. HUME, CATHERINE SHIANG, and JASON J. CHUNG, *Administrative Patent Judges*.

SHIANG, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–5, 7–17, and 19–30, which are all the claims pending and rejected in the application.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] We use "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies Qualcomm Incorporated as the real party in interest. Appeal Br. 3.

[2] Claims 6 and 18 are not before us, as the Examiner has not provided any statutory rejection or objection against those claims. Therefore, we leave it to the Examiner to determine whether claims 6 and 18 are allowable.

STATEMENT OF THE CASE

Introduction

The present invention relates to "techniques for performing multi-layer image fetching using a single hardware image fetcher pipeline of a display processor." Spec. ¶ 4.

> In one example, the disclosure describes a device configured to display frames, the device comprising a layer buffer configured to store two or more independent layers, and a display processor including a single hardware image fetcher pipeline. The single hardware image fetcher pipeline may be configured to concurrently retrieve, from the layer buffer, two or more independent layers, concurrently process the two or more independent layers, and concurrently output, by two or more outputs of the single hardware image fetcher pipeline, the two or more processed independent layers for composition to form one of the frames to be displayed by one or more display units.

Spec. ¶ 6. Claim 1 is exemplary:

> 1. A method of displaying frames, the method comprising:
>
> concurrently retrieving, from a layer buffer and by a single hardware image fetcher pipeline of a display processor, two or more independent layers, the single hardware image fetcher pipeline including a memory dedicated to storing the two or more independent layers for the single hardware image fetcher pipeline;
>
> concurrently processing, after retrieving the two or more independent layers from the memory and by a layer fetcher of the single hardware image fetcher pipeline, the two or more independent layers; and
>
> concurrently outputting, by two or more outputs of the single hardware image fetcher pipeline, the two or more processed independent layers for composition to form one of the frames to be displayed by one or more display units.

Appeal Br. 15 (Claims App.).

References and Rejections[3]

Claims Rejected	35 U.S.C. §	References
1–5, 7–8, 11–17, 19–20, 23–30	103	Croxford (GB 2544357; published May17, 2017)
9–10, 21–22	103	Croxford, MacInnis (US 2011/0280307 A1; published November 17, 2011)

ANALYSIS

Obviousness

On this record, we conclude the Examiner did not err in rejecting claim 1, as discussed below.

We have reviewed and considered Appellant's arguments, but find them to be unpersuasive. To the extent consistent with our analysis below, we adopt the Examiner's findings and conclusions in (i) the action from which this appeal is taken and (ii) the Answer.[4]

Appellant contends Croxford does not teach "the single hardware image fetcher pipeline including a memory dedicated to storing the two or more independent layers for the single hardware image fetcher pipeline," as recited in claim 1. *See* Appeal Br. 9–11; Reply Br. 4–5. For the reasons discussed below, Appellant has not persuaded us of error.

Turning to the Appeal Brief, Appellant's arguments (Appeal Br. 9–11) are unpersuasive because they are not directed to the Examiner's specific

[3] Throughout this opinion, we refer to the (1) Final Office Action dated June 29, 2018 ("Final Act."); (2) Appeal Brief dated November 26, 2018 ("Appeal Br."); (3) Examiner's Answer dated January 18, 2019 ("Ans."); and (4) Reply Brief dated March 14, 2019 ("Reply Br.").

[4] To the extent Appellant advances new arguments in the Reply Brief without showing good cause, Appellant has waived such arguments. *See* 37 C.F.R. § 41.41(b)(2).

findings, as the Examiner cites Croxford's display core—not layer pipelines 24A-24C or shared latency buffers 23—for teaching the claimed "hardware image fetcher pipeline." *See* Final Act. 8; Ans. 15. Further, Appellant's attorney arguments (Appeal Br. 10) are unpersuasive, as Appellant does not provide sufficient objective evidence to support the arguments. *See In re Geisler,* 116 F.3d 1465, 1470 (Fed. Cir. 1997) ("attorney argument [is] not the kind of factual evidence that is required to rebut a prima facie case of obviousness"); *Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977) ("Argument of counsel cannot take the place of evidence lacking in the record.").

In the Answer, the Examiner provides further findings and explanation as to why the disputed limitation is taught by or rendered obvious in light of Croxford's teachings. *See* Ans. 15–16. As discussed below, Appellant fails to persuasively respond to the Examiner's further findings and explanation. Therefore, Appellant fails to show Examiner error. *See In re Baxter Travenol Labs.,* 952 F.2d 388, 391 (Fed. Cir. 1991) ("It is not the function of this court [or this Board] to examine the claims in greater detail than argued by an appellant, looking for [patentable] distinctions over the prior art.").

First, Appellant argues "Claim 1 very clearly recites 'a single hardware image fetcher pipeline,' leaving no room for a construction of the subject matter of claim 1 that would include multiple hardware image fetcher pipelines." Reply Br. 4.

That argument is unpersuasive, because the Examiner cites a single display core from Croxford for teaching the claimed "single hardware image fetcher pipeline." *See* Ans. 15. Further, the Examiner's claim interpretation

is consistent with the Specification, which repeatedly describes a single image fetcher pipeline as one of multiple image fetcher pipelines. *See, e.g.,* Spec. Figs. 1–2; ¶ 40 ("a single hardware image fetcher pipeline of hardware image fetcher pipelines 24), ¶ 45 ("display processor . . . includes image fetchers 24 . . . . Each of image fetchers 24 represent a single hardware image fetcher pipeline configured to perform the techniques described in this disclosure"). As a result, the Examiner properly cites Croxford's single display core, which is one of the two display cores (Croxford Fig. 3), for teaching the claimed "single hardware image fetcher pipeline."

Second, Appellant argues:

> the Examiner has not shown where in the specification a "single hardware image fetcher pipeline" is described as being equivalent to a display processor, nor can the Examiner when claim 1 itself specifically distinguishes between a "single hardware image fetcher pipeline" and a "display processor."

Reply Br. 4.

The above arguments are not directed to the Examiner's specific findings, as the Examiner cites Croxford's display core—not display processor—for teaching the claimed "single hardware image fetcher pipeline." *See* Ans. 15. In fact, Croxford explicitly distinguishes between a display processor and a display core. *See, e.g.,* Croxford Fig. 3 (showing a display processor and a display core are two different components).

Third, Appellant argues:

> The evidence that "single hardware image fetcher pipeline" would have been reasonably understood by a person of ordinary skill in the art to refer to a "display core" is omitted because it is widely understood that the term "processor" as recited by claim 1 is equivalent to a "core" [citing footnote 1].

Reply Br. 4.

> Online Article entitled "CPU definition," updated July 11, 2014, and available at https://techtenns.com/definition/cpu ("For many years, most CPUs only had one processor, but now it is common for a single CPU to have at least two processors or 'processing cores.'").

Reply Br. 4, FN 1.

The above arguments are unpersuasive: regardless of whether it is authoritative, the online article is inapplicable here, because it describes "processing cores"—not Croxford's "core" or "display core" cited by the Examiners.

Fourth, Appellant argues:

> [T]he Examiner's characterization in the Examiner's Answer reproduced above strictly avoids offering any evidence that a "single hardware image fetcher pipeline" would have been reasonably understood by a person of ordinary skill in the art to refer to a "display core."

Reply Br. 4.

Appellant's arguments are unpersuasive because the Examiner is not required to provide the evidence argued by Appellant. It is well settled that:

> [The USPTO] satisfies its initial burden of production by adequately explain[ing] the shortcomings it perceives so that the applicant is properly notified and able to respond. In other words, the PTO carries its procedural burden of establishing a prima facie case when its rejection satisfies 35 U.S.C. § 132, in notify[ing] the applicant . . . [by] stating the reasons for [its] rejection, or objection or requirement, together with such information and references as may be useful in judging of the propriety of continuing the prosecution of [the] application.

Jung, 637 F.3d at 1362 (internal citations and quotation marks omitted). Specifically, the *Jung* Court finds:

> the examiner's discussion of the theory of invalidity (anticipation), the prior art basis for the rejection (Kalnitsky),

> and *the identification of where each limitation of the rejected claims is shown in the prior art reference by specific column and line number was more than sufficient to meet this burden.*

Jung, 637 F.3d at 1363 (emphasis added).

Here, the Examiner's rejection clearly satisfies the requirement of 35 U.S.C. § 132 to establish a prima facie case of unpatentability. The rejection identifies: the theory of unpatentability (obviousness); the prior art basis for the rejection (Croxford); where the disputed limitation is shown in the reference by page and line numbers, plus additional explanation about why the disputed claim limitation is taught by or obvious in light of Croxford's features. *See* Final Act. 8–10, Ans. 15. In short, similar to the Examiner in *Jung*, the Examiner has done "more than sufficient to meet this burden [of establishing the prima facie case]." The burden then shifts to Appellant to rebut the Examiner's prima facie case.

In order to rebut a prima facie case of unpatentability, Appellant must distinctly and specifically point out the supposed Examiner errors, and the specific distinctions believed to render the claims patentable over the applied reference. *See* 37 C.F.R. § 1.111(b). As discussed above in our analysis, Appellant has not carried the burden.

Because Appellant has not persuaded us the Examiner erred, we sustain the Examiner's rejection of independent claim 1, and independent claims 13 and 25 for similar reasons.

We also sustain the Examiner's rejection of corresponding dependent claims 2–5, 7–12, 14–17, 19–24, and 26–30, as Appellant does not advance separate substantive arguments about those claims. *See* 37 C.F.R. § 41.37(c)(1)(iv).

CONCLUSION

We affirm the Examiner's decision rejecting claims 1–5, 7–17, and 19–30 under 35 U.S.C. § 103.

DECISION SUMMARY

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–5, 7–8, 11–17, 19–20, 23–30	103	Croxford	1–5, 7–8, 11–17, 19–20, 23–30	
9–10, 21–22	103	Crowford, MacInnis	9–10, 21–22	
Overall Outcome			1–5, 7–17, 19–30	

FINALITY AND RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

AFFIRMED