UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/825,495	08/13/2015	Carlos Alberto Fernandez	151227/1173-263	8386

115309 7590 09/29/2020

W&T/Qualcomm
106 Pinedale Springs Way
Cary, NC 27511

EXAMINER
BUTLER, SARAI E

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
09/29/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ocpat_uspto@qualcomm.com
patents@wt-ip.com
us-docketing@qualcomm.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CARLOS ALBERTO FERNANDEZ,
JOAB DANIEL HENDERSON, and MICHAEL LOUIS HOBBS

Appeal 2019-003178
Application 14/825,495
Technology Center 2100

Before JOHN A. JEFFERY, SCOTT E. BAIN, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

BAIN, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–28. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

---

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Qualcomm Incorporated. Appeal Br. 1.

BACKGROUND

The Claimed Invention

The invention relates to "computer architectures providing support for random access memory modules." Spec. ¶ 1. Specifically, the invention is directed to "reducing system downtime during memory subsystem maintenance." *Id.* ¶ 5.

Claims 1, 11, 17, and 23 are independent. Claim 1 is illustrative of the invention and the subject matter in dispute, and is reproduced below:

> 1. A computer processing system, comprising:
>
> a plurality of memory sockets, each comprising a gate control and configured to interface with a memory module;
>
> a dedicated non-volatile storage device; and
>
> a computer processor communicatively coupled to the plurality of memory sockets and the dedicated non-volatile storage device;
>
> the *computer processor configured to*:
>
> detect a memory health condition for a memory module interfaced with a memory socket among the plurality of memory sockets;
>
> identify the memory module interfaced with the memory socket of the plurality of memory sockets as a source of the memory health condition;
>
> block access to a memory address range of the memory module based on receiving the indication of the memory module as the source of the memory health condition;
>
> transfer data stored in the memory module to the dedicated non-volatile storage device after the block of the access to the memory address range of the memory module;
>
> *remap* the memory address range of the memory module to the dedicated nonvolatile storage device; and

> *cause voltage gating to be applied to the memory socket using the gate control of the memory socket to render the memory socket inactive after the remap of the memory address range of the memory module to the dedicated nonvolatile storage device.*

Appeal Br. 13 (Claims App.) (emphases added).

References

The references relied upon by the Examiner are:

Name	Reference	Date
Emerson et al. ("Emerson")	US 2002/0129186 A1	Sept. 12, 2002
Lucas et al. ("Lucas")	US 2016/0098328 A1	Apr. 7, 2016
Flynn et al. ("Flynn")	US 2013/0036327 A1	Feb. 7, 2013
Maule et al. ("Maule")	US 2010/0162037 A1	June 24, 2010
Chan	US 2014/0237292 A1	Aug. 21, 2014
Southern et al. ("Southern")	US 2015/0309893 A1	Oct. 29, 2015
Sohn et al. ("Sohn")	US 2013/0227344 A1	Aug. 29, 2013
Cai et al. ("Cai")	US 2015/0363264 A1	Dec. 17, 2015
Strasser et al. ("Strasser")	US 2015/0149817 A1	May 28, 2015
Ackaret et al. ("Ackaret")	US 2014/0089725 A1	Mar. 27, 2014

The Rejections on Appeal

Claims 1, 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, and 26 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, and Flynn. Final Act. 3–7.

Claims 2, 12, 18, and 24 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Maule. Final Act. 8–9.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Chan. Final Act. 9–10.

Claims 6 and 14 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Southern. Final Act. 11–12.

Claims 8 and 16 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Sohn. Final Act. 12.

Claim 10 stands rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Cai. Final Act. 13–14.

Claims 21 and 27 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Strasser. Final Act. 14.

Claims 22 and 28 stand rejected under 35 U.S.C. § 103 as unpatentable over Emerson, Lucas, Flynn, and Ackaret. Final Act. 15.

DISCUSSION

We have reviewed the Examiner's rejections in light of Appellant's arguments presented in this appeal. Arguments that Appellant could have made but did not make in the Briefs are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(iv). For the reasons discussed below, Appellant has not persuaded us of error. We adopt as our own the findings and reasons set forth in the rejections and in the Examiner's Answer, and we provide the following for highlighting and emphasis.

Obviousness Rejection of
Claims 1, 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, and 26

Appellant argues that the Examiner erred in finding the prior art teaches or suggests "caus[ing] voltage gating to be applied to the memory socket . . . *after the remap* of the memory address range of the memory module to the dedicated non-volatile storage device," as recited in claim 1. Appeal Br. 8 (emphasis added); Reply Br. 2–3. Appellant contends that the Examiner relies on the teachings in paragraph 58 of Emerson, which (according to Appellant) only indicates applying voltage gating (e.g., disconnecting power) *before* the memory remapping described therein. Appeal Br. 9. We, however, are unpersuaded of error.

The Examiner relies primarily on Emerson as teaching the disputed limitation, and specifically paragraph 58 of Emerson, reproduced in relevant part below:

> [A] read-modify-write operation is utilized because this operation locks out other bus masters (PCI, AQP, etc.) from accessing the memory bus 105 before the read-modify-write operation has completed. If another bus master writes to the failing RAM 106 module between the portions of the SMM read-modify-write operations to the failing and new RAM 106 modules, the new RAM 106 module will also be written to, thus maintaining data coherency and synchronization between these two RAM 106 modules. Once the read-modify-write transfers of all of the contents of the failing RAM 106 module have been completed, the hot-plug controller 164 disconnects the failing RAM 106 module from the memory bus 105 and system power by means of the FET signal isolation buffers 160 and power FET switches 162 when the memory bus 105 is inactive, and then enables read accesses to the new RAM 106 module so that the next memory read access is serviced by only the new RAM 106 module. Once the failing RAM 106 module has been isolated from the memory bus 105a by the FET signal isolation

> buffers 160, and from the power bus by the power FET switches 162, the failing RAM 106 module may be easily and safely removed from its connector 402 without disturbing normal operation of the computer system 100. Removing the failing RAM 106 module from the memory connector 402 makes this connector 402 available for adding another new RAM 106 module for further replacement . . . .

Emerson ¶ 58; Ans. 16–17.

As seen from the foregoing, Emerson discloses (as Appellant argues) "disconnect[ing] the failing RAM 106 module from . . . system power by means of the FET signal isolation buffers . . . [and] *then* enabl[ing] read accesses to the new RAM 106 module." Emerson ¶ 58 (emphasis added); Appeal Br. 8. In other words, power is disconnected *before* the "read accesses," which Appellant contends would be the "remapping" recited in claim 1 (and thus would not be done "*after* remapping" as recited in claim 1). Appellant's argument, however, misconstrues paragraph 58 of Emerson, and the Examiner's reliance thereon. The "read accesses" in paragraph 58 do not constitute what the Examiner finds to be the "remapping" in Appellant's claim 1. Rather, the "remapping" is the "read-modify-write" operation disclosed in paragraph 58, and the failed memory socket is rendered inactive *after* this operation, just as in claim 1.

Paragraph 57 of Emerson, although not expressly cited by the Examiner, provides the necessary context and meaning of the "read-modify-write" operation further described in paragraph 58. Paragraph 57 describes the "read-modify-write" operation as, essentially, remapping memory modules just as Appellant's Specification does, i.e., rerouting memory access to allow processes to continue uninterrupted while maintenance is performed on a failing memory module. Spec. ¶ 30. Paragraph 57 provides:

> A feature of the embodiments of the invention is *transferring or synchronizing all information contained in the failing RAM 106 module to the new RAM 106 module without disturbing the normal operation of the computer system 100.* The embodiments of the invention do this transferring and synchronizing of information by *enabling writes to both the failing RAM 106 module and the new RAM 106 module*, and reads from only the failing RAM 106 module during the time required to *synchronize* the failing and new RAM 106 modules. Both the failing and new RAM 106 modules respond to the same addresses and are thus activated concurrently. The SMM program running in SMI causes the processor 102 to *execute read-modify-write operations* on the contents of the failing RAM 106 module.

Emerson ¶ 57 (emphases added).

As described above in Emerson's paragraph 58, the failing memory module in Emerson is rendered inactive *after* completion of the "read-modify-write" operation (i.e., the remapping), just as in Appellant's claim 1.

For the foregoing reasons, we are unpersuaded of error regarding the rejection of claim 1. We, therefore, sustain the rejection of claim 1, as well as the rejection of the claims argued as a group with claim 1 (i.e., claims 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, and 26).

Obviousness Rejection of Claims 6 and 14

Appellant argues that the Examiner erred in finding the prior art teaches or suggests "restore power to the memory socket," as recited in dependent claim 6. Appeal Br. 9–10. Appellant contends that the Examiner relies on Southern, which does not teach "restoring" power, because power to the memory modules is never lost in Southern. *Id.*

As the Examiner finds, Southern teaches a "battery" backup or an "auxiliary power supply" for a "failed node." Ans. 18–19; Southern ¶¶ 60–

65. The Examiner finds, and we agree, that one of ordinary skill in the art would understand that the battery or auxiliary power in Southern are merely temporary, backup solutions in the event the main power supply fails, and that once a replacement memory module is received, power must be "restored" to that module in the system disclosed in Southern. Ans. 18–19; Southern ¶ 65. Moreover, Southern's description of applying the auxiliary power supply itself satisfies the "restore power" limitation of claim 6, because the "auxiliary" power was not the original power source for the module. *See id.*

Accordingly, we are not persuaded the Examiner erred in rejecting claim 6, or in claim 14 (which includes the same limitation). We, therefore, sustain the rejection of claims 6 and 14.

Obviousness Rejection of Claims 21 and 27

Appellant argues the Examiner erred in finding the prior art teaches or suggests "maintaining a record of an occurrence of the memory health condition," as recited in claim 21. Appeal Br. 11. Appellant contends the "error history" disclosed in Strasser is not a "memory health condition." *Id.* We, however, are not persuaded of error.

As the Examiner finds, Strasser discloses "error history" as one "aspect[] of non-volatile memory," meaning that Strasser is referring to errors in the *memory*. Ans. 19–20; Strasser ¶ 156. We discern no error in the Examiner's finding that a history of errors is indicative of "memory health," and Appellant does not rebut this finding. Ans. 19–20; *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (claim terms given their "their broadest reasonable interpretation consistent with the

specification"). Moreover, Strasser's disclosure of providing the "history" of such errors necessarily indicates that a "record" was kept.

Accordingly, we are not persuaded the Examiner erred in rejecting claim 21, or in claim 27 (which includes the same limitation). We, therefore, sustain the rejection of claims 21 and 27.

Remaining Rejections

Appellant does not argue the obviousness rejections of the remaining claims separately. Accordingly, for the same reasons as discussed above, we are unpersuaded of error regarding the obviousness rejections of claims 2, 3, 4, 8, 10, 12, 16, 18, 22, 24, and 28. We sustain the rejections of those claims.

CONCLUSION

We affirm the Examiner's decision rejecting claims 1–28.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, 26	103	Emerson, Lucas, Flynn	1, 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, 26	
2, 12, 18, 24	103	Emerson, Lucas, Flynn, Maule	2, 12, 18, 24	
3, 4	103	Emerson, Lucas, Flynn, Chan	3, 4	
6, 14	103	Emerson, Lucas, Flynn, Southern	6, 14	
8, 16	103	Emerson, Lucas, Flynn, Sohn	8, 16	

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
10	103	Emerson, Lucas, Flynn, Cai	10	
21, 27	103	Emerson, Lucas, Flynn, Strasser	21, 27	
22, 28	103	Emerson, Lucas, Flynn, Ackaret	22, 28	
Overall Outcome			1–28	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

AFFIRMED