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EXAMINER	
PARIKH, KALPIT	

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PHIL JOSEPH BOSTLEY III and
JAYA PRAKASH SUBRAMANIAM GANASAN

Appeal 2019-003173
Application 14/626,913
Technology Center 2100

Before SCOTT E. BAIN, MICHAEL T. CYGAN, and
STEPHEN E. BELISLE, *Administrative Patent Judges*.

BAIN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–3, 5–10, 12–19, and 21–34. Claims 4, 11, and 20 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Qualcomm Incorporated. Appeal Br. 3.

BACKGROUND

The Claimed Invention

The invention relates to computer processors, and more specifically, to "cache coherence bus traffic control based on a processor's role." Spec. ¶ 1. Claims 1, 8, 17, and 26 are independent. Claim 1 is illustrative of the invention and the subject matter in dispute, and is reproduced below:

> 1. A method for routing a coherence request to one or more caches in a computing system, the method comprising:
>
> determining one or more transaction attributes for a cache coherence transaction from a requesting processor, wherein the one or more transaction attributes includes at least *a secure root identifier (NS) for identifying a secure root* in the requesting processor, wherein the *cache coherence transaction was initiated by the secure root*;
>
> identifying a cachability domain and/or shareability domain based on the one or more transaction attributes; and
>
> routing the cache coherence transaction to one or more caches in the identified cachability domain and/or shareability domain.

Appeal Br. 13 (Claims Appendix) (emphases added).

References

The references relied upon by the Examiner are:

Name	Reference	Date
Heller, Jr. et al. ("Heller")	US 2004/0268044 A1	Dec. 30, 2004
Nguyen et al. ("Nguyen")	US 2011/0055844 A1	Mar. 3, 2011
Fullerton	US 2011/0126265 A1	May 26, 2011

The Rejections on Appeal

Claims 1–3, 5, 6, 8–10, 12, 13, 15–19, 21, 22, 24–29, and 31–34 stand rejected under 35 U.S.C. § 103 as unpatentable over Heller and Fullerton. Final Act. 2–5.

Claims 7, 14, 23, and 30 stand rejected under 35 U.S.C. § 103 as unpatentable over Heller, Fullerton, and Nguyen. Final Act. 5–6.

DISCUSSION

We have reviewed the Examiner's rejections in light of Appellant's arguments presented in this appeal. On the record before us, we cannot sustain the Examiner's rejections.

Appellant argues the Examiner erred in finding the prior art teaches or suggests transaction attributes that include a "secure root identifier (NS) for identifying a secure root in the requesting processor," and a "cache coherence transaction . . . *initiated by the secure root*," as recited in claim 1. Appeal Br. 6–8 (emphasis added); Reply Br. 2–4. According to Appellant, the Examiner relies on Fullerton's teaching of a "trusted domain identifier" as satisfying the "secure root" limitation of claim 1. Appellant argues, however, that the trusted domain identifier cannot be the "secure root" of claim 1 because the trusted domain identifier does not (among other things) "initiate" the cache coherence transaction (or even identify what initiated the cache coherence transaction). Appeal Br. 6. Appellant also argues the Examiner erred in finding a rationale to combine the references. We need not address Appellant's rationale to combine argument, because we are persuaded the Examiner erred in finding the prior art teaches a "cache coherence transaction . . . initiated by the secure root."

The Examiner relies on Fullerton's description of "partitions" as teaching or suggesting the disputed claim limitations. Ans. 4–5 (citing Fullerton Fig. 3 (element 302), ¶ 13); *see also* Final Act. 3 (citing Fullerton Fig. 4 (element 402), ¶¶ 22, 24). Figure 3 is a flowchart depicting steps to "configure plurality of isolated domains" and "assign each isolated domain a unique domain identifier." Fullerton Fig. 3. Step 302 states, "[a]ssociate resources with each isolated domain and store as permissions to access physical addresses of resources." *Id.* Figure 4, another flow chart, states at step 402 "[h]ardware compares domain identifier of instruction with permissions." Paragraph 13 states, a "processor core may be logically partitioned into a plurality of domains," and paragraphs 22 and 24 describe "access[ing] . . . shared resources." *Id.* at ¶¶ 13, 22, 24.

The Examiner does not explain, on this record, how any of the foregoing discussion teaches a secure root identifier *that initiates a cache coherence transaction*, as recited in claim 1. Even if we accept the Examiner's finding that the domain identifiers of Fullerton are "secure root identifiers" (claim 1), the Examiner has not identified any teaching as to the "initiate" limitation of claim 1. As Appellant argues, the Examiner's reliance on the "domain" identified in paragraph 13 of Fullerton (and subsequently discussed in the other passages cited by the Examiner) refers merely "to peripherals, memory space, etc., none of which are described as initiat[ing]" the "transaction" (operation or code) recited in claim 1. Appeal Br. 7.

Accordingly, we are persuaded the Examiner erred in rejecting claim 1. For the same reasons, we are persuaded of error regarding the remaining claims on appeal, all of which include the same disputed

limitation (or depend from a claim that does). We, therefore, do not sustain the obviousness rejections of claims 1–3, 5–10, 12–19, and 21–34.

CONCLUSION

We reverse the Examiner's decision rejecting claims 1–3, 5–10, 12–19, and 21–34.

SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–3, 5, 6, 8–10, 12, 13, 15–19, 21, 22, 24–29, 31–34	103	Heller, Fullerton		1–3, 5, 6, 8–10, 12, 13, 15–19, 21, 22, 24–29, 31–34
7, 14, 23, 30	103	Heller, Fullerton, Nguyen		7, 14, 23, 30
Total Outcome				1–3, 5–10, 12–19, 21–34

REVERSED