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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SIMON SIU-SING CHAN, LEI XUE, YOUSEOK SUH, AMOL RAMESH JOSHI, HIDEHIKO SHIRAIWA, HARPREET SACHAR, KUO-TUNG CHANG, CONNIE PIN CHIN WANG, PAUL R. BESSER, SHENQING FANG, MENG DING, TAKASHI ORIMOTO, WEI ZHENG, and FRED TK CHEUNG

Appeal 2019-003047
Application 11/958,646
Technology Center 2800

Before DONNA M. PRAISS, MICHELLE N. ANKENBRAND, and JEFFREY R. SNAY, *Administrative Patent Judges.*

PRAISS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 11, 12, 15–19, 21, 22, 26, 28, 29, 31, and 32. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] Appellant is the applicant, Cypress Semiconductor Corporation, which, according to the Appeal Brief, is the real party in interest. Appeal Brief ("Appeal Br.") filed Aug. 15, 2018, 1.

STATEMENT OF THE CASE[2]

The invention "relates generally to integrated circuit systems and more particularly to integrated circuit systems having a memory system." Spec. ¶ 2. The Specification discloses "Flash" memory systems with a floating gate architecture undergo a size reduction of key features with new semiconductor processes. Spec ¶ 6. According to the Specification, this causes an undesired increase in programming time and a decrease in data retention. *Id.* The Specification discloses that charge trapping architectures provide improved scalability compared to floating gate architectures. *Id.* ¶ 7. One such architecture is a silicon-oxide-nitride-oxide semiconductor (SONOS), which traps a charge in a nitride layer. *Id.* Integrating memories with other devices or functions involves trade-offs such as reliability, cost, and overall integrated device yield. *Id.* ¶ 8.

The Specification discloses a need for an integrated circuit system with memory integration that provides low cost manufacturing, improved yields, improved programming performance, and improved data density of memory in a system. *Id.* ¶ 9. In view of this, the Specification discloses an integrated circuit system including a substrate with a core region and a periphery region, a charge storage stack over the substrate in the core region, a gate stack with a stack header having a metal portion over the substrate in the periphery region, and a memory system with the stack header over the charge storage stack. *Id.* 12. Appellant's Figure 4 is reproduced below with our annotations.

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[2] Our Decision also refers to the Specification ("Spec.") filed Dec. 18, 2007, the Examiner's Final Office Action ("Final Act.") dated Feb. 15, 2018, the Examiner's Answer ("Ans.") dated Jan. 11, 2019, and the Reply Brief ("Reply Br.") filed Mar. 8, 2019.

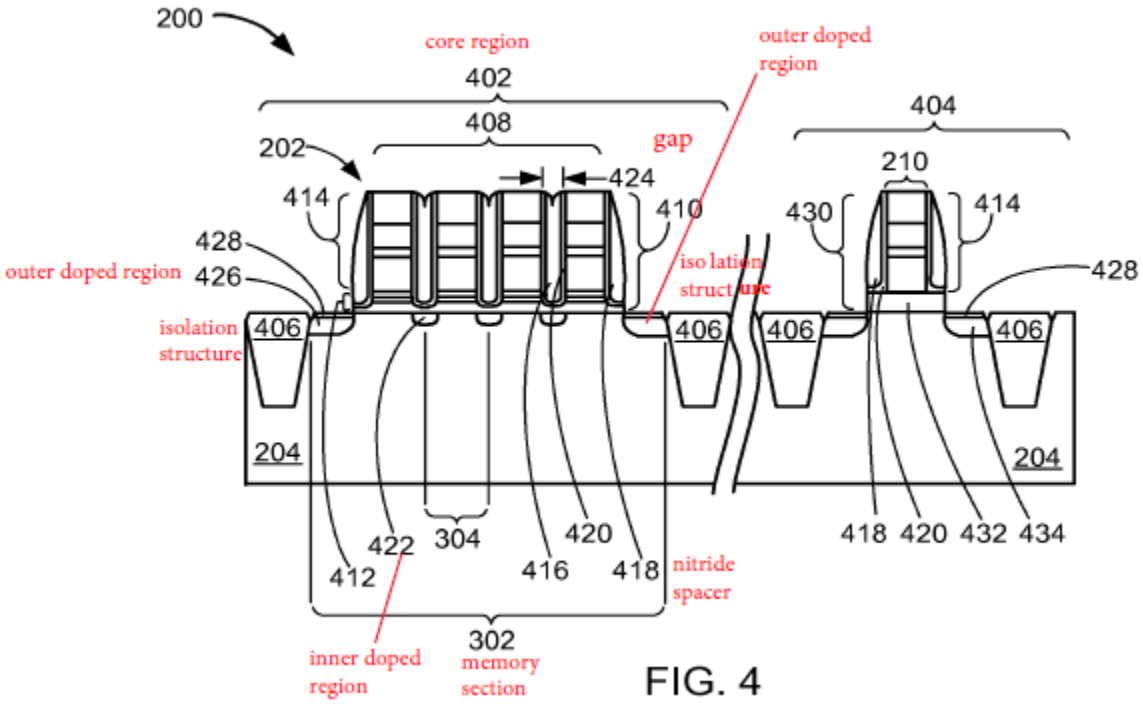

FIG. 4

Annotated Figure 4 above is a cross-sectional view of Appellant's integrated circuit system 200 illustrating core region 402, periphery region 404, and memory section 302 having a plurality of memory stacks 410. Spec. ¶¶ 16, 31–33. Inner doped region 422 and outer doped region 428 may function as a source or drain of memory section 302. *Id.* ¶ 34. Gap filler 416 between adjacent memory stacks 410 may be nitride filler and spacer 418 along sidewall 420 at the ends of memory section 302 may be nitride spacer. *Id.* ¶ 33. Outer doped regions 428 are located between spacers 418 and isolation structures 406. *Id.* ¶ 34.

Claim 11, reproduced below from the Claims Appendix to the Appeal Brief, is illustrative (disputed limitations are italicized).

11. An integrated circuit system comprising:

a substrate having a core region and a periphery region;

a gate stack comprising a gate stack header, the gate stack header comprising a first metal portion formed from a

> first metal layer, the gate stack disposed over the substrate in the periphery region; and
>
> a non-volatile memory system comprising silicon-oxide-nitride-oxide (SONOS) memory cells disposed in a memory section of the core region, the memory cells comprising memory stacks disposed between first and second isolation structures in the core region, wherein the memory stacks comprise memory stack headers disposed over multi-layer charge storage stacks disposed over the substrate in the core region, wherein the memory stack headers of the memory cells comprise a semi-conducting portion disposed above the multi-layer charge storage stacks, a transition portion comprising a transition metal nitride disposed above the semiconducting portion, and a second metal portion disposed above the transition portion, wherein a respective gap between each pair of adjacent memory stack headers is lined by a dielectric lining and filled by a dielectric tiller, and wherein the second metal portion of the memory stack headers is formed from the same first metal layer as the first metal portion of the gate stack header;
>
> *wherein a first outer doped region in the core region extends between a nitride spacer on a first end of the memory section and the first isolation structure, and a second outer doped region in the core region extends between another nitride spacer on a second end of the memory section and the second isolation structure*;
>
> *wherein one or more inner doped regions are located in the substrate under one or more respective gaps between the memory stacks, wherein the one or more inner doped regions have different doping than the first outer doped region and the second outer doped region*.

Independent claim 21 recites "[a]n integrated circuit system comprising," among other things, a substrate, a dielectric liner, a gate stack, and a non-volatile memory system having outer doped regions and one or more inner

doped regions similar to those recited in claim 11. Each remaining claim on appeal depends from claim 11 or claim 21.

ANALYSIS

We review the appealed rejections for error based upon the issues Appellant identifies and in light of the arguments and evidence produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (*cited with approval in In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("[I]t has long been the Board's practice to require an applicant to identify the alleged error in the examiner's rejections.")). After considering the argued claims in light of the case law presented in this Appeal and each of Appellant's arguments, we are not persuaded of reversible error in the Examiner's rejections.

Rejection 1: Obviousness

The Examiner rejects claims 11, 12, 15, 21, 22, 26, 28, 29, 31, and 32 under 35 U.S.C. § 103(a) as unpatentable over Goda[3] in view of Lee,[4] Mokhlesi,[5] Willer,[6] and Kang.[7] Final Act. 3–13.

Appellant argues the claims together. Appeal Br. 6–9.[8] Therefore, we confine our discussion to claim 11, which we select as representative.

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[3] Goda et al., US 2005/0093047 A1, published May 5, 2005 ("Goda").
[4] Lee, US 2006/0261398 A1, published November 23, 2006 ("Lee").
[5] Mokhlesi et al., US 2005/0157549 A1, published July 21, 2005 ("Mokhlesi").
[6] Willer et al., US 6,686,242 B2, issued February 3, 2004 ("Willer").
[7] Kang et al., US 2007/0034938 A1, published February 15, 2007 ("Kang").
[8] For independent claim 21, Appellant relies on the same argument presented for claim 11. Appeal Br. 8. Appellant's assertions that claims 12, 15, 22,

Claims 12, 15, 21, 22, 26, 28, 29, 31, and 32 stand or fall with claim 11. *See* 37 C.F.R. § 41.37(c)(1)(iv).

The Examiner finds Goda discloses, among other things, a substrate having a core region, a gate stack, and a non-volatile memory system having silicon-oxide-nitride-oxide (SONOS) memory cells disposed in a memory section of the core region. Final Act. 3–4. The Examiner finds Goda's memory cells include memory stacks, the core region of the substrate includes a first outer doped region and a second outer doped region, and the substrate also includes one or more inner doped region under one or more respective gaps between the memory stacks. *Id.* at 4–5. Goda's Figure 1 is reproduced below.

26, 28, 29, 31, and 32 introduce one or more additional recitations that render them patentable (*id.* at 9) do not amount to "separate" arguments, because Appellant merely refers to the additional claim limitations followed by a generic denial that the cited prior art teaches or suggests the claimed method. We and our reviewing court have long held that such "argument" does not merit separate consideration. *See*, *e.g.*, *In re Lovin*, 652 F.3d 1349, 1357 (Fed. Cir. 2011) ("[W]e hold that the Board reasonably interpreted Rule 41.37 to require more substantive arguments in an appeal brief than a mere recitation of the claim elements and a naked assertion that the corresponding elements were not found in the prior art.").

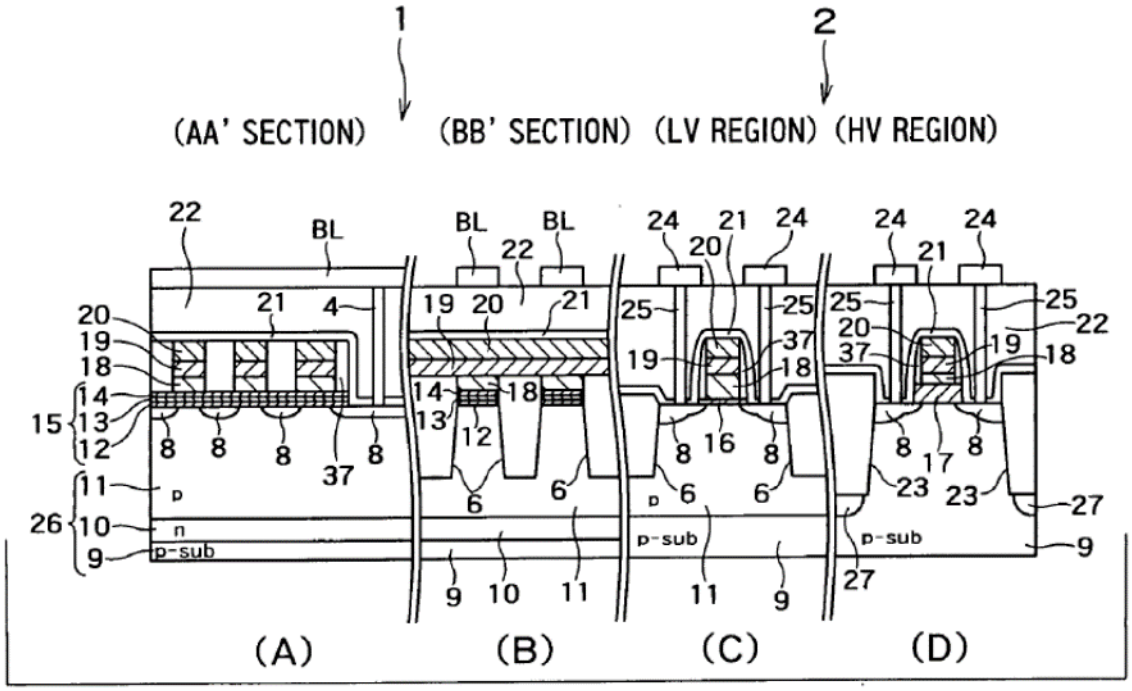


FIG. 1

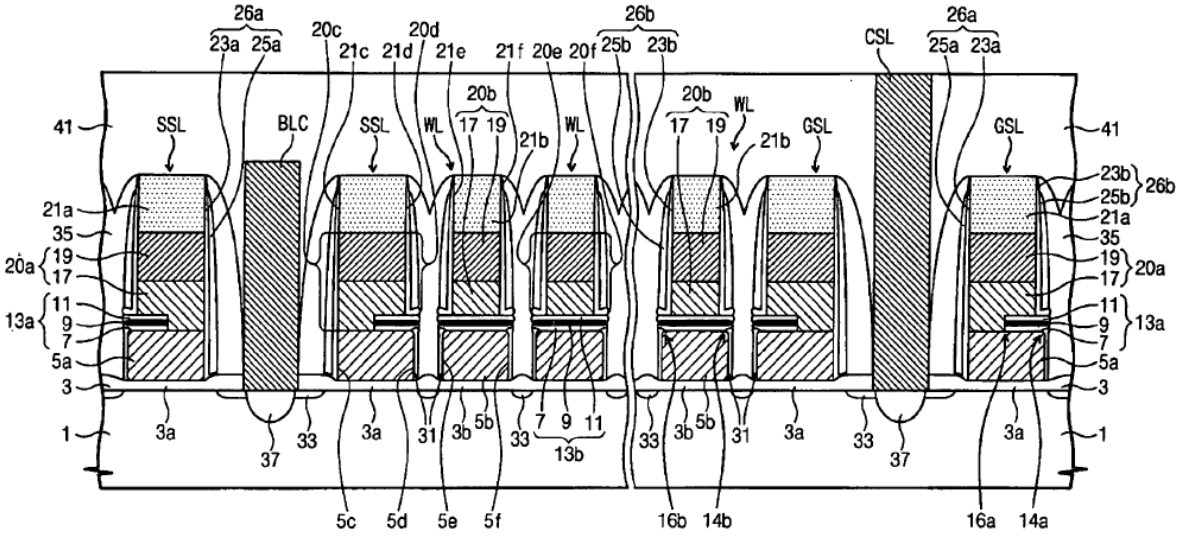
Goda's Figure 1 illustrates a sectional view of a semiconductor device.

Goda discloses that a semiconductor device includes memory cell device 1 and peripheral circuit portion 2. Goda ¶¶ 6, 27, 138, 140. Memory cell device 1 has substrate 26 and includes bit lines BL and word lines (not depicted in Figure 1). *Id.* ¶¶ 28, 149. Bit line contacts 4 are formed on source and drain regions 8 of bit lines BL and source line contacts (not depicted in Figure 1) are formed in regions of bit line BL adjacent to GSL signal line (not depicted in Figure 1). *Id.* ¶¶ 28, 184. Memory cell device 1 also includes ONO layer 15 composed of tunnel insulating layer 12, charge accumulating layer 13, and block insulating layer 14. *Id.* ¶ 34. In addition, memory cell device 1 has first gate electrode 18 and second gate electrode 19 in a memory cell region. *Id.* ¶ 145.

The Examiner finds Lee discloses a first outer doped region extending between a spacer on a first end of a memory section and a first isolation structure and a second outer doped region extending between another spacer on a second end of the memory section and a second isolation structure, as claim 11 requires. Final Act. 5–6. The Examiner concludes it would have been obvious to modify Goda to include Lee's outer doped regions to provide electrical isolation between a core region and peripheral regions and to allow each region to be confined in an optimal field as Lee teaches. *Id.* at 6 (citing Lee ¶ 50).

The Examiner finds Kang discloses one or more inner doped regions that have different doping than first and second outer doped regions. *Id.* at 4–5, 7. The Examiner concludes it would have been obvious to modify Goda to have different doping for the outer doped regions, as in Kang, to reduce contact resistance for the source and bit line contacts. *Id.* (citing Kang Fig. 2 and related text). Kang's Figure 2 is reproduced below.

Fig. 2



Kang's Figure 2 illustrates a sectional view of a NAND-type non-volatile memory device.

Kang discloses gate insulators 3a and 3b, floating gates 5a and 5b, and mask patterns 21a and 21b stacked on semiconductor substrate 1. Kang ¶¶ 25–26. According to Kang, lightly doped drain region 33 may be formed in substrate 1 adjacent to and between adjacent wordlines WL, string selection lines SSL, ground selection lines GSL, and/or common source lines CSL. *Id.* ¶ 43. Heavily doped regions 37 may also be formed between adjacent string selection lines SSL and ground selection lines GSL. *Id.* ¶ 45.

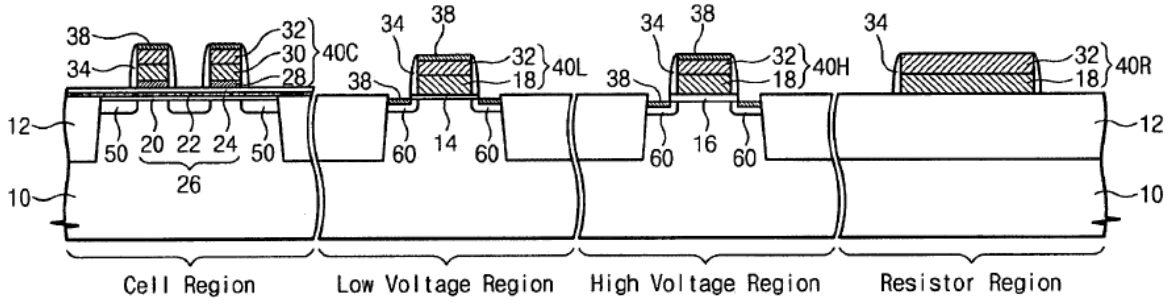
Appellant contends the Examiner cites regions 8 in Figure 1 of Goda as both outer doped regions and one or more inner doped regions, however, Goda's region 8 is the same and does not provide different doping, as claim 11 requires. Appeal Br. 6–7. Appellant also argues Kang's regions 37 do not extend between a nitride spacer on the end of a memory section and an isolation structure, as claim 11 requires, and Kang's regions 33 are directly adjacent regions 37 without any spacer. *Id.* at 7–8. According to Appellant, Lee, Willer, and Mokhlesi do not cure the alleged deficiencies of Goda and Kang. *Id.* at 8.

In response to Appellant's arguments, the Examiner explains that Goda is not relied upon to disclose or suggest claim 11's requirement that one or more inner doped regions have different doping than first and second outer doped regions. Ans. 3–4 (explaining that Appellant's argument is against Goda individually instead of the proposed combination). Specifically, the Examiner finds Kang's lightly doped drain regions 33 correspond to one or more inner doped regions and Kang's heavily doped regions 37 correspond to outer doped regions having different doping.

Ans. 4–6; *see* Final Act. 7. The Examiner explains that Goda's source and drain regions 8 are first and second outer doped regions that do not have different doping, but are regions to which electrical contact is made (i.e., contacts 3, 4 depicted in Goda's Figure 46). Ans. 5; Final Act. 4. The Examiner further explains that Kang's heavily doped regions 37 are also regions to which electrical contact is made (i.e., via contacts BLC and CSL as shown in Kang's Figure 2 above). Ans. 5.

In response to Appellant's arguments that Kang's regions 37 do not extend between a nitride spacer on the end of a memory section and an isolation structure, as claim 11 requires, and that Kang's regions 33 are directly adjacent regions 37 without any spacer (Appeal Br. 7–8), the Examiner explains that Lee discloses outer doped regions that extend in this way. Ans. 7–8. Regarding the claim term "extends between," the Examiner determines an outer doped region need only exist in a region intermediate a nitride spacer and isolation structure and an outer doped region need not begin at a nitride spacer and end at an isolation structure based on the dictionary definitions of "extend" and "between." *Id.* at 8–9 (citing Collins English Dictionary, 12th ed., 2014). Lee's Figure 1A is reproduced below.

Fig. 1A



Lee's Figure 1A shows a sectional view of a non-volatile memory device.

Lee discloses a cell region that includes multi-layer charge-storage insulation layer 26 on which gate electrode 40C is formed. Lee ¶ 35. Lee's device further includes substrate 10 having source and drain regions 50 and field isolation layer 12. *Id.* Lee teaches sidewall spacers 34 on the sidewalls of gate electrodes 40C and that field isolation layers 12 confine a plurality of active regions in substrate 10. *Id.* ¶¶ 45, 50. The Examiner finds source / drain region 50 on the left of one cell gate electrode 40C functions as a first outer doped region at a first end of a memory section that extends between a spacer (i.e., sidewall spacer 34) and a first isolation structure (i.e. field isolation layer 12 on the left). The Examiner similarly finds source / drain region 50 on the right of another cell gate electrode 40C functions as a second outer doped region at a second end of the memory section that extends between a spacer (i.e., sidewall spacer 34) and a second isolation structure (i.e., field isolation layer 12 on the right). Final Act. 5–6.

In the Reply Brief, Appellant contends the Examiner's Answer does not address Appellant's argument regarding Goda, Appellant did not argue against the references individually, the Examiner relied upon Goda as teaching one or more inner doped regions and outer doped regions, and the Examiner's reasoning presents a new ground of rejection. Reply Br. 1–4.

Appellant's arguments are not persuasive of error because they do not address the Examiner's rejection, but, rather, attack the applied references individually. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references . . . [The reference] must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re*

Keller, 642 F.2d 413, 425 (CCPA 1981)). The Examiner sufficiently explained that Goda discloses first and second outer doped regions (i.e., source / drain regions 8 at ends of memory string) and inner doped regions (i.e., source / drain regions 8 between memory stack headers), but Goda does not disclose that these regions have different doping. Final Act. 4–5. The Examiner relied on Kang's regions with different doping (i.e., lightly doped drain regions 33 and heavily doped regions 37) and explained why it would have been obvious to modify Goda's regions in view of Kang's teachings. *Id.* at 7; Ans. 4–6. The record supports that Examiner's finding as to Kang's disclosure. Kang ¶ 46.

Appellant argues the Examiner's reasoning is confusing because it maps inner doped regions to Kang's reference numerals 31 and 33. Reply Br. 3. This argument is unpersuasive because Appellant misinterprets Kang's Figure 2. Kang discloses "thermal oxide layers 31 covering the sidewalls of the string selection lines SSL, the ground selection lines GSL and the wordlines WL." Kang ¶ 44. Therefore, numeral 31 in Figure 2 does not reference the regions in substrate 1 between wordlines WL or between a wordline WL and a ground selection line GSL in Figure 2, but, rather, the layer on the vertical sidewalls of those lines, such as along the sidewalls of floating gates 5a, 5b. The Examiner's second arrow from the left on page 6 of the Answer refers to an unlabeled lightly doped drain region 33 in Kang's Figure 2. In addition, the third arrow from the left on page 6 of the Answer clearly refers to lightly doped drain region 33, which is consistent with the Examiner's findings in the rejection.

Appellant asserts the Examiner's interpretation misrepresents Appellant's position, Appellant has not stated a meaning for "extends

between," the Examiner's interpretation is based on conjecture, and the interpretation is a new ground of rejection. Reply Br. 5–7. These arguments are also unpersuasive. The Examiner's interpretation appears to be in response to Appellant's arguments in the Appeal Brief, the Examiner cites a dictionary definition to support the interpretation, and Appellant's arguments dispute the Examiner's interpretation without identifying a reversible error in that interpretation.

To the extent Appellant argues that Kang's structure must be incorporated into Goda's configuration, "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981) (citations omitted). Here, the applied references support the Examiner's findings and the Examiner sufficiently explains how the combination of the applied references would have suggested the claimed invention. Based on the cited record in this Appeal, Appellant's arguments do not identify a reversible error in the Examiner's rejection of claim 11.

In the Reply Brief, Appellant also contends the Examiner's rationale for modifying Goda's regions 8 to reduce contact resistance lacks factual evidence. Reply Br. 4. This is a new argument in the Reply Brief that Appellant did not present in the Appeal Brief. Therefore, we need not consider it absent a showing of good cause, which is lacking here. 37 C.F.R. § 41.41(b)(2). Nonetheless, Kang's disclosure supports the Examiner's rationale for modifying Goda because Kang teaches "[t]he heavily doped regions 37 serve to reduce contact resistance between the common source

line(s) CSL and the semiconductor substrate 1, and between the bitline contact(s) BLC and the semiconductor substrate 1." Kang ¶ 46. As discussed above, the Examiner explains how it would have been obvious to apply this advantage to Goda's source / drain regions 8, which have contacts 3, 4. Ans. 4–5.

For these reasons and those the Examiner provides, we uphold the Examiner's rejection of 11, 12, 15, 21, 22, 26, 28, 29, 31, and 32 under 35 U.S.C. § 103(a) as obvious over Goda, Lee, Mokhlesi, Willer, and Kang.

Rejection 2: Obviousness

The Examiner rejects claims 16–19[9] under 35 U.S.C. § 103(a) as being unpatentable over Goda in view of Lee, Mokhlesi, Willer, and Kang and further in view of Hopper[10] for the reasons provided on pages 13–15 of the Final Office Action.

Appellant argues Hopper does not cure the deficiencies discussed above with regard to the rejection of claim 11 and asserts each of claims include additional limitations that are patentable. Appeal Br. 8–9. As discussed above, there are no deficiencies in the rejection of claim 11 for Hopper to cure based on the record cited in this Appeal. In addition, Appellant's arguments merely cite additional limitations of the dependent claims with a generic denial that the applied references teach or suggest the limitations or cure the deficiencies of the principal references. Such

[9] Appellant canceled claim 23 in an amendment filed August 15, 2018. The Examiner entered the claim amendment in an Advisory Action dated October 5, 2018.
[10] Hopper et al., US 6,406,960 B1, issued June 18, 2002 ("Hopper").

arguments do not merit separate consideration. *See*, *e.g.*, *In re Lovin*, 652 F.3d at 1357.

For these reasons, and those the Examiner provides, we uphold the Examiner's rejections of claims 16–19 under 35 U.S.C. § 103(a) as obvious over Goda, Lee, Mokhlesi, Willer, Kang, and Hopper.

DECISION

Upon consideration of the record, and for the reasons given above, in the Final Office Action, and in the Examiner's Answer, the decision of the Examiner rejecting claims 11, 12, 15, 21, 22, 26, 28, 29, 31, and 32 under 35 U.S.C. § 103(a) as obvious over Goda in view of Lee, Mokhlesi, Willer, and Kang and rejecting claims 16–19 under 35 U.S.C. § 103(a) as being unpatentable over Goda in view of Lee, Mokhlesi, Willer, and Kang and further in view of Hopper is *affirmed*.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	References/Basis	Affirmed	Reversed
11, 12, 15, 21, 22, 26, 28, 29, 31, 32	103(a)	Goda, Lee, Mokhlesi, Willer, Kang	11, 12, 15, 21, 22, 26, 28, 29, 31, 32	
16–19	103(a)	Goda, Lee, Mokhlesi, Willer, Kang, Hopper	16–19	

Claims Rejected	35 U.S.C. §	References/Basis	Affirmed	Reversed
Overall Outcome			11, 12, 15–19, 21, 22, 26, 28, 29, 31, 32	

AFFIRMED