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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/612,485	02/03/2015	Steven Noyes	67036-791PUS1; 79630US01	7637

26096 7590 09/01/2020

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ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
09/01/2020	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEVEN NOYES

Appeal 2019-003009
Application 14/612,485
Technology Center 2100

Before CARL W. WHITEHEAD JR., ADAM J. PYONIN, and MICHAEL J. ENGLE, *Administrative Patent Judges.*

PYONIN, *Administrative Patent Judge.*

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's rejection. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse and enter new grounds of rejection.

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Hamilton Sundstrand Corporation. Appeal Br. 1.

STATEMENT OF THE CASE

Introduction

The Application is directed "to a method of testing electronic equipment for single upset event resistance," in which single upset events (SEUs) "are changes of state caused by ions or electromagnetic radiation striking an electric device, which can cause an error or malfunction." Spec. ¶¶ 1, 2. Claims 1–15 are pending; claims 1 and 8 are independent. Appeal Br. 10–12. Claim 1 is reproduced below for reference:

> 1. A system for simulating an event, comprising:
> a memory system;
> a parity generator/validator; and
> a fault injector, the fault injector configured to inject bits at an address in the memory system when the parity generator/validator is in an disabled state.

References and Rejections

The Examiner relies on the following prior art:

Name	Reference	Date
Wisor	US 5,606,662	Feb. 25, 1997
Leonard	US 2008/0046136 A1	Feb. 21, 2008
Asaad	US 2011/0219208 A1	Sept. 8, 2011
Cox	US 2012/0084628 A1	Apr. 5, 2012
Dan	US 2012/0144244 A1	June 7, 2012

Claims 1–15 are rejected under 35 U.S.C. § 101 as being patent ineligible. Final Act. 4.

Claim 4 is rejected under 35 U.S.C. § 112(a) as failing to comply with the enablement requirement. Final Act. 6.

Claims 1–6, 8, 9, and 12–15 are rejected under 35 U.S.C. § 103 as obvious in view of Dan, Cox, and Wisor. Final Act. 7.

Claim 7 is rejected under 35 U.S.C. § 103 as obvious in view of Dan, Cox, Wisor, and Leonard. Final Act. 10.

Claims 10 and 11 are rejected under 35 U.S.C. § 103 as obvious in view of Dan, Cox, Wisor, and Asaad. Final Act. 10.

ANALYSIS[2]

We have reviewed the Examiner's rejections in light of Appellant's arguments. We discuss each of the grounds of rejection in turn, below.

Patent Eligibility

The Examiner determines the claims are patent ineligible under 35 U.S.C. § 101, because "the claimed invention is directed to a judicial exception (i.e., a law of nature, a natural phenomenon, or an abstract idea) without significantly more." Final Act. 4; *see Alice Corp. v. CLS Bank Int'l*, 573 U.S. 208, 217–218 (2014) (describing the two-step framework "for distinguishing patents that claim laws of nature, natural phenomena, and abstract ideas from those that claim patent-eligible applications of those concepts").

Prior to the filing of Appellant's Reply Brief—but after the filing of the Appeal Brief and mailing of the Final Action and Examiner's Answer–the U.S. Patent and Trademark Office (USPTO) published revised guidance

[2] Appellant challenges the Examiner's construction of claims 1–7 as reciting a means plus function limitation. *See* Appeal Br. 3, 4. We do not reach this construction issue because whether these claims recite a means plus function limitation is not germane to our analysis herein.

on the application of § 101 ("Guidance").[3] *See* Guidance documents including 2019 Revised Patent Subject Matter Eligibility Guidance Notice, 84 Fed. Reg. 50 (Jan. 7, 2019) ("Notice"); *see also* USPTO, October 2019 Update: Subject Matter Eligibility ("October Update") at 17 (available at https://www.uspto.gov/sites/default/files/documents/peg_oct_2019_update.pdf). "All USPTO personnel are, as a matter of internal agency management, expected to follow the [G]uidance." Notice, 84 Fed. Reg. at 51; *see also* October Update at 1.

> Under the Guidance, we first look to whether the claim recites:
>
> (1) any judicial exceptions, including certain groupings of abstract ideas (i.e., mathematical concepts, certain methods of organizing human activity such as a fundamental economic practice, or mental processes) ("Step 2A, Prong One"); and
>
> (2) additional elements that integrate the judicial exception into a practical application (see MPEP § 2106.05(a)–(c), (e)–(h) (9th ed. Rev. 08.2017, Jan. 2018)) ("Step 2A, Prong Two").

Notice, 84 Fed. Reg. at 52–55. Only if a claim (1) recites a judicial exception and (2) does not integrate that exception into a practical application, does the Office then look, under Step 2B, to whether the claim:

> (3) adds a specific limitation beyond the judicial exception that is not "well-understood, routine, conventional" in the field (see MPEP § 2106.05(d)); or
>
> (4) simply appends well-understood, routine, conventional activities previously known to the industry, specified at a high level of generality, to the judicial exception.

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[3] We note Appellant does not refer to the Notice in the Reply Brief. *See* Reply Br. 1, 2. Appellant does not waive any arguments against the eligibility rejection, however, because "[i]t is the rejection under § 101, and not any alleged failure to comply with the [Notice], that is reviewed by the Patent Trial and Appeal Board." October Update at 17.

Notice, 84 Fed. Reg. at 52–56.

We find the Examiner's eligibility rejection is in error. Even if claim 1 recites a judicial exception under Prong One of the Guidance, we determine the claim integrates such exception into a practical application. Specifically, claim 1 recites an additional element of "a fault injector, the fault injector configured to inject bits at an address in the memory system when the parity generator/validator is in [a] disabled state." Appeal Br. 10. This "allows the fault to be injected into the electronic device" (Spec. 16) to "[p]redict[] the impact of SEUs [which] becomes increasingly important as the complexity of electronics increases, and as they become more compact" (Spec. ¶ 3). The recitation of this element is a technical solution (injecting bits into a memory) to a technical problem (determining the effect of radiation on an electronic device). *See* Spec. ¶¶ 1–3, 9, 18. The claim, therefore, "reflects an improvement in the functioning of a computer, or an improvement to other technology or technical field." Notice, 84 Fed. Reg. at 55; *see* MPEP § 2106.06(a) (Explaining an example of a technical improvement when "[t]he claim was not simply the addition of general purpose computers added post-hoc to an abstract idea, but a specific implementation of a solution to a problem in the software arts.").

Based on the foregoing, we determine claim 1 "improves technology, [and] the claim imposes meaningful limits on any recited judicial exception, and the claim [is] eligible under the [Notice] at least at Step 2A Prong Two." October Update at 11. We do not sustain the Examiner's patent eligibility

rejection of independent claim 1, independent claim 8 which recites somewhat similar limitations,[4] or the claims dependent thereon.

Enablement

The Examiner concludes that claim 4 does not comply with the enablement requirement, because the claim recites a "random event generator," and "[t]he specification merely states that software/logic is used to generate the random event. One having ordinary skill in the art would need to know at least the algorithm or method used to generate a random event in order to implement it." Final Act. 6–7.

Appellant argues the claim is enabled:

> generating a random event is well-known in the art and one of ordinary skill would know how to do so, especially in view of the disclosure that the random event generator software/logic is provided by the SEU injector and that the random event generator determines when faults should be injected.

Appeal Br. 6.

We find the Examiner errs. "To satisfy the enablement requirement of 35 U.S.C. 112(a), the specification must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." Examining Computer-Implemented Functional Claim Limitations for Compliance with 35 U.S.C. 112, 84 Fed. Reg. 57, 62 (Jan. 7, 2019). "Not everything necessary to practice the invention need be disclosed," however, as "a specification need not disclose what is well

[4] "The § 101 patent-eligibility inquiry is only a threshold test. Even if an invention qualifies as a process, machine, manufacture, or composition of matter, in order to receive the Patent Act's protection the claimed invention must also satisfy 'the conditions and requirements of this title.' § 101." *Bilski v. Kappos*, 561 U.S. 593, 602 (2010).

known in the art." *Id*. (internal quotations omitted). Appellant's Specification explains that "the software/logic for a random event generator . . . , which performs a timekeeper function to determine when faults should be injected," governs "[h]ow often faults are injected [and] simulates different real-world conditions." Spec. ¶¶ 11, 13.

We agree with Appellant that random event generators are well known in the art, and one of ordinary skill in the art would have been able to make and use the invention without undue experimentation. *See* Appeal Br. 6. In contrast, the Examiner has not provided any concrete support for the conclusion that the claims are not enabled. *Cf. McRO, Inc. v. Bandai Namco Games Am. Inc*., 959 F.3d 1091, 1103–04 (Fed. Cir. 2020) (The "observations merely state the conclusion that the claims are too broad and the specification's discussion is too narrow. The observations do not justify the conclusion with any concrete support."). Accordingly, we find the Examiner has not established a lack of enablement for the random event generator limitation of claim 4. We do not sustain the Examiner's rejection under 35 U.S.C. § 112(a).

Obviousness

Appellant argues the Examiner's obviousness rejection is in error, because "[t]he Examiner has failed to make a *prima facie* case of obviousness at least because the Examiner did not explain why one of ordinary skill would modify Dan with Cox and Wisor." Appeal Br. 7. Appellant asserts "the Examiner has provided no reason why one of ordinary skill would have modified Dan in view of Cox to disable a parity generator/validator in view of [Wisor]. The Examiner only makes the

conclusory statement that the combination is 'an obvious variation.'" *Id*. at 8 (quoting Final Act. 8).

We are persuaded the Examiner errs. "[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 418 (2007). Establishing obviousness requires "determin[ing] whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue," and "in many cases, this analysis should be made explicit." *Id*.

Here, the Examiner's proffered reason to combine the teachings of the cited references is that "one having ordinary skill in the art would find this modification to be an obvious variation." Final Act. 8. Given an opportunity to elaborate in the Answer, the Examiner further states "there is sufficient explanation given in the rejections" of the Final Action, and that "enabling/disabling a parity mechanism would be obvious to try in view of the other references." Ans. 6. These statements merely articulate the conclusion of obviousness. The Examiner has not identified a recognized need or problem to be solved, shown there was a reasonable expectation of success in modifying the references' teachings, or otherwise provided any reason explaining why one of ordinary skill would have combined Dan, Cox, and Wisor in the manner claimed. *See* Ans. 6; Reply Br. 3.

We are persuaded the Examiner has not established claim 1 is obvious in view of the combined teachings of Dan, Cox, and Wisor. The Examiner rejects independent claim 8 for the same reasons as provided for claim 1. *See* Final Act. 9. Accordingly, we do not sustain the Examiner's

obviousness rejection of the independent claims, or the rejections of the claims dependent thereon.

NEW GROUND OF REJECTION

Pursuant to our authority under 37 C.F.R. § 41.50(b), we enter new grounds of rejection and separately reject independent claim 8 under 35 U.S.C. § 102(a)(1) as anticipated by Wisor.

Claim 8 recites the following:

> 8. A method of injecting a fault, comprising:
> determining an address;
> disabling a parity generator/validator;
> determining a bit; and
> writing the bit to the address.

We find Wisor anticipates these limitations. Wisor discloses selective parity disabling, such that the parity generator/validator will be disabled (as claimed) for certain memory. *See* Wisor Abstract, Figs. 2–5. Specifically, Wisor discloses determining an address, because Wisor writes to the memory banks in a specified order "to determine which of the DRAM banks 206 support parity." Wisor 5:43–44; *see also* Fig. 4 (step 416 (increment bank)). Wisor disables the parity generator/validator, as claimed. *See* Wisor 6:14–16 ("If the parity error register was set, thus indicating that the DRAM bank 0 does not support parity, the configuration register 302A is cleared."); *cf*. 6:40–44 ("[T]he selective enable unit 218 causes parity to be generated and checked by the memory control unit 204 depending upon those banks which support parity."). Wisor further discloses determining a bit and writing the bit to the address. *See* Wisor Fig. 4, 6:23–24 ("Subsequently, a

similar write operation using a known data pattern is performed for DRAM bank 1."). Accordingly, Wisor anticipates the steps recited by claim 8.

Separately, we note claim 8 does not preclude a step of enabling parity after the step of disabling. Nor does claim 8 require a specific order to the performance of the recited steps—the recited step of disabling may reasonably occur before or after the recited determining step. *See Baldwin Graphic Sys., Inc. v. Siebert, Inc*., 512 F.3d 1338, 1345 (Fed. Cir. 2008) ("[A]lthough a method claim necessarily recites the steps of the method in a particular order, as a general rule the claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order."); *see* MPEP § 2111.01(II). Wisor also broadly but reasonably discloses the method of claim 8, accounting for the disabling step occurring prior to the determining step:

> *Each write parity generator 214 is selectively enabled depending upon the stored information within the configuration register 302 of selective enable unit 218*. Similar to the embodiment of FIG. 2, during normal operation, an enable bit is generated for data being stored within those DRAM banks that support parity. If a particular bank does not support parity as determined by the 20 system BIOS, the configuration bit 302A-302D associated with that bank will be cleared. Accordingly, a parity bit will not be generated. When a read of the data occurs, *the selective enable 218 unit either enables or disables the read parity generator 216*. It is noted that the memory control unit 25 500 is configured such that if parity checking is disabled, the original parity signal will match the new parity signal, and thus the output of exclusive OR gate 220 will be low. Accordingly, the parity error bit is not set.

Wisor 7:14–29 (emphases added). Wisor's selective enable unit 218 will disable the parity generators and parity checking (i.e. the recited parity generator/validator) for memory that does not support parity. *See* Wisor Fig. 3. Wisor's system is used for writing data to memory (i.e., the recited

determining an address, determining a bit, and writing a bit to the address) once parity support is determined. *See* Wisor 4:60–64 ("Address and control logic circuit 210 is configured to drive appropriate address and bank select signals to the plurality DRAM banks 206" which are "well known functions."); 6:39–40 ("subsequent operations of the computer system (i.e., normal operation)"). Accordingly, Wisor discloses the recited limitations.

Claim 8 includes, as a preamble, a "method of injecting a fault." These terms are not recited further in the claim, which recites writing to a memory and disabling a parity device. The preamble "merely gives a descriptive name to the set of limitations in the body of the claim that completely set forth the invention." *IMS Tech., Inc. v. Haas Automation*, Inc., 206 F.3d 1422, 1434 (Fed. Cir. 2000). Therefore, we give no weight to the preamble of claim 8. *See Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) ("[A] preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.") (internal quotations marks and citation omitted). Even given weight, however, we find that Wisor anticipates "injecting a fault." Wisor discloses parity checking is used to determine errors written into memory: "[p]arity is the simplest form of error detection," and a "parity error is detected upon reading the data byte and verifying the parity of that word." Wisor 1:27. Wisor discloses that the step of writing a bit to an address is a method of introducing an error (i.e., injecting a fault), because error checking is needed. *See* Wisor, Abstract ("[T]he advantages attained by parity error checking will be realized for the DRAM banks that support parity.").

For the above reasons, we find claim 8 is anticipated by Wisor. We note the Patent Trial and Appeal Board is a review body, rather than a place of initial examination. We have rejected independent claim 8 based on our authority under 37 C.F.R. § 41.50(b). We have not, however, reviewed the remaining claims to the extent necessary to determine whether those claims are unpatentable under 35 U.S.C. §§ 102 or 103. We leave it to the Examiner to ascertain whether the remaining claims should be rejected over Wisor, alone or in combination with additional prior art.

DECISION SUMMARY

Claims Rejected	35 U.S.C. §	Reference(s)/ Basis	Affirmed	Reversed	New Ground
1–15	101	Eligibility		1–15	
4	112	Enablement		4	
1–6, 8, 9, 12–15	103	Dan, Cox, Wisor		1–6, 8, 9, 12–15	
7	103	Dan, Cox, Wisor, Leonard		7	
10, 11	103	Dan, Cox, Asaad		10, 11	
8	102	Wisor			8
Overall Outcome				1–15	8

TIME PERIOD FOR RESPONSE

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of

the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. . . .

Further guidance on responding to a new ground of rejection can be found in the Manual of Patent Examining Procedure § 1214.01.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED; 37 C.F.R. § 41.50(b)