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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PAUL L. RODGERS and TIMOTHY R. LAROCCA

Appeal 2019-002471
Application 15/842,193
Technology Center 2800

Before MICHELLE N. ANKENBRAND, CHRISTOPHER C. KENNEDY, and MONTÉ T. SQUIRE, *Administrative Patent Judges*.

ANKENBRAND, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision[2] finally rejecting claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Northrup Grumman Systems Corporation as the real party in interest. Appeal Brief, filed January 2, 2019 ("Appeal Br.") 3.

[2] Final Action, mailed October 12, 2018 ("Final Act.").

STATEMENT OF THE CASE

Background

The subject matter on appeal relates to a driver circuit that can generate a switch control signal and control a switch. Specification, filed Dec. 14, 2017 ("Spec.") ¶¶ 1, 3–4. The driver circuit includes a source amplifier and an active load. *Id.* ¶ 1. The source amplifier has an amplifying field effect transistor (FET) device. *Id.* At the amplifying FET device, a control signal is input to a gate terminal and an amplified control signal is output at a drain terminal. *Id.* ¶ 9. The active load has a self-biasing load FET device. *Id.* ¶ 1. A self-biasing line that includes a resistor connects a source terminal and a gate terminal of the self-biasing load FET device. *Id.* ¶ 10. A power source is coupled to a drain terminal of the load FET device. *Id.*

According to the Specification, the driver circuit generates a switch control signal with very fast pulse edges and a large voltage swing. *Id.* ¶ 3. This provides an improved driver circuit that can turn a switch on and off quickly for high-speed, high-voltage applications. *Id.*

Of the appealed claims, claims 1, 9, and 17 are independent. Claim 1 is representative of the subject matter on appeal, and reproduced below:

> 1. A driver circuit comprising:
>
> a source amplifier including an amplifying field effect transistor (FET) device having a drain terminal, a gate terminal and a source terminal, said amplifying FET device receiving a control signal at its gate terminal and outputting an amplified control signal at its drain terminal; and
>
> an active load including a load FET device having a drain terminal, a gate terminal and a source terminal, said drain terminal of the load FET device being coupled to a power supply, said source terminal of the load FET device being

coupled to the drain terminal of the amplifying FET device, and said source and gate terminals of the load FET device being electrically coupled by a self-biasing line, said active load including a load resistor provided in the self-biasing line.

Appeal Br. 15 (Claims App'x).

The References

Miura	US 6,829,152 B2	Dec. 7, 2004
Damiano	US 4,616,305	Oct. 7, 1986

Möench et al., *Quasi-normally-off GaN Gate Driver for High Slew-Rate D-Mode GaN-on-Si HEMTs*, Proceedings of the 27th Int'l Symposium on Power Semiconductor Devices & IC's (May 10–14, 2015), 373

The Rejections

The Examiner maintains the following rejections on appeal:

1. Claims 1, 5–9, and 13–17 under 35 U.S.C. § 102 as anticipated by Miura.

2. Claims 1, 5–9, and 13–17 under 35 U.S.C. § 102 as anticipated by Damiano.

3. Claims 2–4, 10–12, and 18–20 under 35 U.S.C. § 103 as unpatentable over Miura.

4. Claims 2, 3, 10, 11, 18, and 19 under 35 U.S.C. § 103 as unpatentable over Damiano.

Final Act. 2–6; Examiner's Answer, dated Jan. 28, 2019 ("Ans.") 3–7.

OPINION

After considering the evidence presented in this Appeal and each of Appellant's contentions, we are persuaded that Appellant identifies

reversible error with respect to the Examiner's rejection of claims 1–20. We reverse the Examiner's rejection of those claims for the reasons below.

Anticipation and Obviousness Rejections – Miura

In rejecting claim 1 as anticipated by Miura, the Examiner finds that Miura discloses a driver circuit including, among other things, a source amplifier including an amplifying FET device that receives a control signal at a gate terminal and outputs an amplified control signal at a drain terminal, and an active load including a load FET device coupled to a power supply and the amplifying FET device, where the load FET device source terminal and gate terminal are electrically coupled by a self-biasing line. Final Act. 2–3; Ans. 4–5 (both citing Miura, Fig. 14). The Examiner maps the recited source amplifier to transistor T2 of Miura's Figure 14. Final Act. 2; Ans. 4.

Appellant argues that Miura's transistor T2 is a switching transistor and does not output an amplified control signal at its drain terminal. Appeal Br. 9. Appellant asserts that the circuit shown in Miura's Figure 14 is an evaluation circuit for evaluating "the recovery characteristic of the diode Df1 when the transistor T2 operates as a load-driving transistor and the transistor T1 operates as a flywheel diode." *Id.* at 8 (citing Miura, 9:14–20).

In response to Appellant's argument, the Examiner finds that the transistor T2 will inherently provide an amplified control signal at its drain terminal due to the 30V supply voltage applied across the driver circuit shown in Figure 14. Ans. 9.

Appellant's argument is persuasive.

> "To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The

> mere fact that a certain thing may result from a given set of circumstances is not sufficient."

In re Robertson, 169 F.3d 743, 745 (Fed. Cir. 1999) (internal citations and quotations omitted). Here, the Examiner does not adequately address the limitation "said amplifying FET device . . . outputting an amplified control signal at its drain terminal" in claim 1.

In the Final Action, the Examiner maps the recited source amplifier to transistor T2 of Miura's Figure 14 and finds that Miura discloses an amplifying FET device that outputs an amplified control signal at a drain terminal. Final Act. 2–3; Ans. 4–5. But the Examiner does not provide any explanation or direct us to any record evidence demonstrating how transistor T2 provides an amplified control signal at a drain terminal. *See* Final Act. 2–3; Ans. 4–5. Further, although the Examiner finds that the transistor T2 inherently provides an amplified control signal based on its connection to a 30V power supply, the Examiner does not cite any evidence to support this finding. *See* Ans. 9. For example, the Examiner does not point to any record evidence indicating that a 30V power supply connected to a transistor necessarily causes the transistor to output an amplified signal. *See id.* Therefore, the Examiner does not sufficiently explain how the output of an amplified control signal is necessarily present in transistor T2 of Miura's Figure 14. Accordingly, we reverse the Examiner's rejection of claim 1.

Independent claims 9 and 17 recite a substantially similar limitation to claim 1, and the Examiner relies on the same rationale to address that limitation in claims 9 and 17. Final Act. 3; Ans. 5; *see* Appeal Br. 16–17 (Claims App'x) (claims 9 and 17). The Examiner also rejects dependent claims 5–8 and 13–16 as anticipated by Miura, and dependent claims 2–4,

10–12, and 18–20 as having been obvious over Miura. Final Act. 3, 5; Ans. 5, 7. In the obviousness rejection, the Examiner additionally cites to Möench.[3] Final Act. 5; Ans. 7. However, the Examiner does not provide any additional explanation or evidence to remedy the deficiency discussed above. *See* Final Act. 3, 5; Ans. 5, 7. Therefore, we reverse the Examiner's rejections of claims 2–20 for the same reasons that we reverse the Examiner's rejection of claim 1.

Anticipation and Obviousness Rejections – Damiano

In rejecting claim 1 as anticipated by Damiano, the Examiner finds that Damiano discloses a driver circuit including, among other things, a source amplifier including an amplifying FET device that receives a control signal at a gate terminal and outputs an amplified control signal at a drain terminal, and an active load including a load FET device coupled to a power supply and the amplifying FET device, where the load FET device source terminal and gate terminal are electrically coupled by a self-biasing line. Final Act. 3–4; Ans. 5–6 (both citing Damiano, Fig. 1). The Examiner maps the recited amplifying FET device to transistor Q2 in Damiano's Figure 1. Final Act. 4; Ans. 6.

Appellant argues that transistor Q2 is a switching transistor and does not output an amplified control signal at its drain terminal. Appeal Br. 10–11. Appellant asserts that the circuit shown in Figure 1 is a reversing H-

[3] The Examiner finds that Miura does not specifically disclose that its amplifying and load transistors are GaN depletion mode devices, as some of the dependent claims require. Final Act. 5. Nevertheless, the Examiner determines that such devices would have been obvious to the ordinarily skilled artisan because it was "well-known" in the art to form driver circuits using GaN depletion mode devices as Möench evidences. *Id.*

drive system that provides power to drive an inductive load with two power circuits, where transistor Q2 is part of a first power circuit. *Id.* at 10.

In response to Appellant's argument, the Examiner finds that transistor Q2 will inherently provide an amplified control signal at its drain terminal because "the control signal IN1 is a small signal control input and the high voltage power supply +DC on line 2 will cause the control signal IN1 to be amplified at the drain terminal of transistor Q2." Ans. 11.

Appellant's argument is persuasive, as we find that the Examiner does not adequately address the limitation "said amplifying FET device . . . outputting an amplified control signal at its drain terminal" in claim 1. In the Final Action, the Examiner maps the recited source amplifier to transistor Q2 of Damiano's Figure 1, and finds that Damiano discloses an amplifying FET device that outputs an amplified control signal at a drain terminal. Final Act. 4; Ans. 6. But the Examiner does not provide any explanation or direct us to any record evidence showing how transistor Q2 provides an amplified control signal at a drain terminal. *See* Final Act. 4; Ans. 6. Further, although the Examiner finds that transistor Q2 inherently provides an amplified control signal based on the control signal IN1 being a small signal control input and the high voltage power supply +DC, the Examiner does not cite any evidence to support this finding. *See* Ans. 9. For example, the Examiner does not provide any citation supporting the statement that control signal IN1 is a small signal control input. *See id.* Nor does the Examiner point to any record evidence indicating that a high voltage supply connected to a transistor necessarily causes the transistor to output an amplified signal. *See id.* Therefore, the Examiner does not sufficiently explain how the output of an amplified control signal is

necessarily present in transistor Q2 of Damiano's Figure 1. Accordingly, we reverse the Examiner's rejection of claim 1.

As discussed above, independent claims 9 and 17 recite a substantially similar limitation as claim 1. The Examiner relies on the same rationale to address that limitation in claims 9 and 17. Final Act. 4; Ans. 6. The Examiner also rejects dependent claims 5–8 and 13–16 as anticipated by Damiano, and dependent claims 2, 3, 10, 11, 18, and 19 as having been obvious over Damiano. Final Act. 4–6; Ans. 6–7. In the obviousness rejection, the Examiner additionally cites to Möench as evidence that it was well known to form driver circuits using GaN depletion mode transistors. Final Act. 6; Ans. 7. However, the Examiner does not provide any additional explanation or evidence to remedy the deficiency discussed above. *See* Final Act. 4–6; Ans. 6–7. Accordingly, we reverse the Examiner's rejections of claims 2, 3, 5–11, and 13–19 for the same reasons that we reverse the Examiner's rejection of claim 1.

CONCLUSION

We reverse the Examiner's rejections of claims 1–20 under 35 U.S.C. § 102 and 35 U.S.C. § 103.

In summary:

Claims Rejected	35 U.S.C. §	Reference/ Basis	Affirmed	Reversed
1, 5–9, 13–17	102	Miura		1, 5–9, 13–17
1, 5–9, 13–17	102	Damiano		1, 5–9, 13–17
2–4, 10–12, 18–20	103	Miura		2–4, 10–12, 18–20
2, 3, 10, 11, 18, 19	103	Damiano		2, 3, 10, 11, 18, 19

Overall Outcome				1–20

REVERSED