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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEFAN MACHEINER and MARKUS DINKEL

Appeal 2019-002393
Application 15/075,266
Technology Center 2800

BEFORE CATHERINE Q. TIMM, JEFFREY R. SNAY, and
MICHAEL G. McMANUS, *Administrative Patent Judges*.

McMANUS, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant¹ seeks review of the Examiner's decision to reject claims 1–7, 22, and 23. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

¹ We use the word “Appellant” to refer to “applicant” as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Infineon Technologies AG. Appeal Br. 3.

CLAIMED SUBJECT MATTER

The present application generally relates to a packaged semiconductor device that includes a leadframe, a semiconductor die attached to the leadframe, and an encapsulation material encapsulating the semiconductor die and a portion of the leadframe. Spec. ¶ 3.

Figures 1A and 1C of the Application are reproduced below.

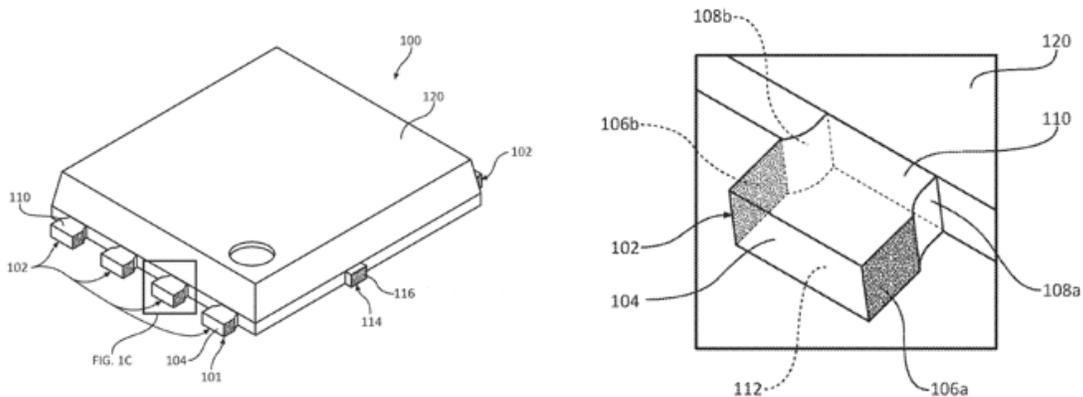


Figure 1A (left) shows a top perspective view of packaged semiconductor device 100 including leads 102 having plated end faces 104. *Id.* ¶ 15.

Figure 1C (right) is an enlarged view of a lead 102. *Id.* ¶ 18. Figure 1C shows “plated end face 104, first and second unplated sidewalls 106a and 106b, and first and second plated sidewalls 108a and 108b, respectively.” *Id.* The Specification teaches that unplated “sidewalls 106a and 106b are formed when leadframe 101 is singulated from a leadframe strip.” *Id.*

Plating is considered desirable as it enhances wettability of the solder used to adhere the lead to a land or circuit board. *Id.* ¶ 14. More specifically, the Specification teaches that “semiconductor devices as described herein include leads having a fully plated end face that enables

solder wetting to provide a solder fillet,” *id.*, and “the plating enables solder wetting of end face 104,” *id.* ¶ 20. The presence of plating on the end face permits automated optical inspection (AOI) to determine whether solder wetting between a lead and a circuit board is acceptable. *Id.* ¶ 14.

Claim 1 is illustrative of the subject matter on appeal and is reproduced below with certain limitations bolded for emphasis:

1. A semiconductor device comprising:

a leadframe comprising a first main face disposed entirely in a first plane and a second main face opposite to the first main face disposed entirely in a second plane, the leadframe comprising leads wherein each lead comprises a fully plated planar end face extending between **an unplated first sidewall and an unplated second sidewall opposite to the first sidewall**, the end face and the first and second sidewalls of each lead perpendicular to the first and second main faces;

a semiconductor die attached to the leadframe; and

an encapsulation material encapsulating the semiconductor die and a portion of the leadframe and forming a plurality of side surfaces of the semiconductor device,

wherein each lead extends from a side surface and comprises a plated first sidewall between the unplated first sidewall and the encapsulation material and a plated second sidewall between the unplated second sidewall and the encapsulation material, and

wherein, **except for the unplated first and second sidewalls of each lead, all surfaces of the leadframe are plated**, including portions of the leadframe encapsulated with the encapsulation material, including a portion to which the semiconductor die is attached.

Appeal Br. 10 (Claims App.) (emphasis added).

REFERENCES

The Examiner relies upon the following prior art:

Name	Reference	Date
Tsuji et al. (“Tsuji”)	US 5,521,432	May 28, 1996
Sato et al. (“Sato”)	US 2006/0138615 A1	June 29, 2006
Madrid et al. (“Madrid”)	US 2010/0164078 A1	July 1, 2010
Celaya et al. (“Celaya”)	US 2010/0187663 A1	July 29, 2010
Hess et al. (“Hess”)	US 2011/0108965 A1	May 12, 2011

REJECTIONS²

The Examiner maintains the following rejections:

1. Claims 1–3, 5–7, 22 and 23 are rejected under 35 U.S.C. § 103 as being unpatentable over Celaya in view of Sato, Tsuji, and Madrid. Final Act. 2–9.
2. Claim 4 is rejected under 35 U.S.C. § 103 as being unpatentable over Celaya in view of Sato, Tsuji, and Madrid, and further in view of Hess. *Id.* at 9–10.

DISCUSSION

Rejection 1. The Examiner rejects claims 1–3, 5–7, 22, and 23 as obvious over Celaya in view of Sato, Tsuji, and Madrid. Final Act. 2–9. Appellant presents arguments seeking the reversal of the rejection of claim

² In the Final Office Action dated Dec. 15, 2017 (“Final Act.”), the Examiner rejected claims 9–11 and 13 as obvious. This rejection was rendered moot by amendment cancelling such claims entered Jan. 28, 2019.

1. Appeal Brief filed June 18, 2018 (“Appeal Br.”) 5–8. Appellant further argues that the rejection of claims 2, 3, 5–7, 22, and 23 should be reversed in view of their dependency on claim 1. *Id.* at 8. Accordingly, the rejection of claims 2, 3, 5–7, 22, and 23 will stand or fall with that of claim 1. *See* 37 C.F.R. § 41.37(c)(1)(iv).

In support of the rejection, the Examiner finds that Celaya teaches most of the structural limitations of claim 1. Final Act. 3. The Examiner further finds, however, that Celaya does not teach a “fully plated end face extending between an unplated first sidewall and an unplated second sidewall opposite to the first sidewall” as well as certain other limitations. *Id.* at 3. Rather, the leads of Celaya are fully plated. *See, e.g.*, Celaya ¶ 27, Fig. 3.

The Examiner additionally finds that the secondary reference, Sato, teaches a “leadframe comprising leads wherein each lead comprises a fully plated end face extending between an unplated first sidewall and an unplated second sidewall opposite to the first sidewall, the end face and the first and second sidewalls of each lead perpendicular to the first and second main faces.” *Id.* at 3–4. Figure 8 of Sato is reproduced below.

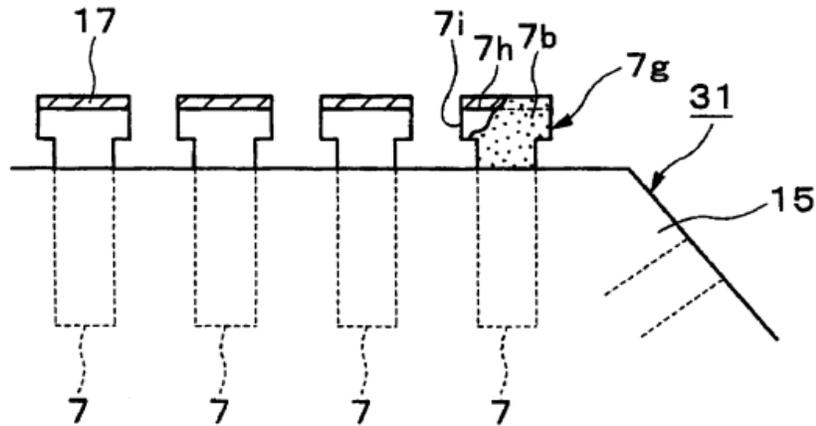


Figure 8 of Sato shows semiconductor package 31 having “leads 7, plated layers 17, fully plated end face 7h, [and] unplated sidewalls 7g/i.” Final Act. 4; *see also* Sato ¶ 64. Sato teaches that, in view of its teaching regarding plating, “it is possible to improve the anti-wetting ability and to increase the overall area available for the solder 25 attached to the lead 7.” Sato ¶ 57.

The Examiner finds that a person of ordinary skill in the art would have had reason to combine the teachings of Celaya and Sato as it would permit “a plurality of lead frames to be formed at the same time and plating said leads before cutting the leads from the lead frame strip and will avoid the additional step of forming a second plating layer after cutting the leadframe to create a fully plated end face.” Final Act. 5.

Appellant argues that the rejection is made in error. Appeal Br. 4–8. More specifically, Appellant argues that the Examiner’s findings run “counter to the teachings of Cel[a]ya which teaches that all faces of the leads are plated in order to maximize solder wettability of the leads.” *Id.* at 7. Appellant similarly argues that one of ordinary skill who sought to combine

the teachings of the cited references would have followed Celaya's teachings to plate all surfaces thereby requiring an additional process step and eliminating the efficiency cited by the Examiner. *Id.*

“[A] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.” *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006).

“When prior art contains apparently conflicting references, the Board must weigh each reference for its power to suggest solutions to an artisan of ordinary skill” and, in so doing, “consider the degree to which one reference might accurately discredit another.” *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

Here, Sato teaches an embodiment where the lead is soldered to a land of a printed circuit board. Sato ¶ 56. In this regard, Sato teaches that

The recess is subjected to plating so as to increase **the overall area of solder for establishing electric connection between the lead and a board (or a substrate)**. That is, it is possible to **improve the joining strength** between the lead and solder without increasing the overall area of the backside of each lead, which is exposed to the terminal surface (or lower surface) of the molded resin body.

Sato ¶ 11 (emphasis added); *see also id.* ¶ 65. That is, Sato teaches that the arrangement depicted in Figure 8, above, “improve[s] the joining strength” between the lead and solder. This teaching is not directly contrary to Celaya.

Celaya teaches that semiconductor devices “are typically manufactured” by a process where “[e]lectrically conductive material 40 is absent from end surfaces 26 of leadframe leads 12” due to singulation (such

as cutting). Celaya ¶ 26. Celaya further teaches that a drawback of having portions of the leadframe exposed is that “[t]he exposed portions may not wet during surface mount processes leading to corrosion creep during extreme atmospheric conditions such as those within an automotive engine compartment” and further that “the exposed portions of the leadframes may form unreliable solder joints.” *Id.* ¶ 2.

Thus, Celaya teaches that not plating the entirety of a lead may risk corrosion in extreme environments and the formation of unreliable solder joints. Sato teaches that by plating end face 7h in the manner disclosed therein, “it is possible to reliably increase the joining strength between the lead 7 and the solder” without also plating the lead sidewalls. Sato ¶ 65. If the second plating step of Celaya were omitted, this would leave *end surfaces* 26 exposed, not sidewalls. Sato, however, teaches to leave *sidewalls* 7g and 7i exposed. Accordingly, the teachings of Celaya (regarding exposed end surfaces) are not be in direct conflict with those of Sato (regarding exposed sidewalls). Both Celaya and Sato focus on assuring that lead end surfaces are plated.

Further, Celaya’s concern that unplated regions may be subject to corrosion in extreme environments presumably would be lessened for semiconductor packages intended to be used under less extreme conditions. Similarly, those of ordinary skill in the art likely would prioritize a single step process, such as that taught by Sato, over Celaya’s multi-step plating in certain circumstances. Both the process described as “typical” in Celaya where end walls are exposed (Celaya ¶ 2) and the process of Sato where sidewalls are exposed intentionally (Sato, Fig. 8) are taught to be conventional and suitable for manufacture of leadframe leads.

Considering all of the foregoing and weighing the teachings of the references, *see Young*, 927 F.2d at 591, we determine that Appellant has not shown error in the Examiner's determination that one of ordinary skill in the art would have had reason to combine the teachings of Celaya and Sato in rejecting claim 1.

Appellant briefly argues that Celaya "teaches away" from the Examiner's proposed hypothetical combination on the same basis. Appeal Br. 5, 7. Prior art may teach away if it "criticize[s], discredit[s], or otherwise discourage[s] the solution claimed." *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). "[A]ll of the relevant teachings of the cited references must be considered in determining what they fairly teach to one having ordinary skill in the art." *In re Mercier*, 515 F.2d 1161, 1165 (CCPA 1975); *Para-Ordnance Mfg., Inc. v. SGS Imps. Int'l, Inc.*, 73 F.3d 1085, 1090 (Fed. Cir. 1995) (disclosures that arguably teach away "must be weighed alongside" disclosures that teach "the propriety of" making the proposed modification). "[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes." *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012); *see also In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) ("A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use."). "The fact that the motivating benefit comes at the expense of another benefit . . . should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another. Instead, the benefits, both lost and gained, should be weighed against one another." *Winner Int 'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000).

Weighing the teachings of the references, we determine that Appellant has not shown that the teachings of Celaya would have guided a person of ordinary skill in the art away from the exposed sidewall conformation of Sato. Celaya's suggestion that exposed endwalls can impart certain disadvantages relative to full plating does not "teach away" from the functional and step-saving design of Sato's unplated sidewalls.

Appellant argues that the rejection of claims 2, 3, 5-7, 22, and 23, which depend from claim 1, should be reversed on the same basis as argued for claim 1. Appeal Br. 8. In view of the foregoing, we determine not to reverse the rejection of these claims.

Rejection 2. The Examiner rejects claim 4 as obvious over Celaya in view of Sato, Tsuji, and Madrid, and further in view of Hess. Final Act. 9-10. Appellant argues that the rejection of claim 4 should be reversed for the same reasons set forth with regard to claim 1. As we have not found such arguments to be persuasive, we determine not to reverse the rejection of claim 4.

CONCLUSION

The Examiner's rejections are affirmed.

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1-3, 5-7, 22, and 23	103	Celaya, Sato, Tsuji, Madrid	1-3, 5-7, 22, 23	
4	103	Celaya, Sato, Tsuji, Madrid, Hess	4	
Overall Outcome			1-7, 22, 23	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED