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LAM, YEE F

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEFANIA GANDAL, NOAM EFRATI, and ADI KATZ[1]

Appeal 2019-002383
Application 14/655,168
Technology Center 2400

Before JOHN A. JEFFERY, JAMES R. HUGHES, and JOHN A. EVANS, *Administrative Patent Judges*.

EVANS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of Claims 1, 3, 4, 7–12, and 14–16, which constitute all the claims pending in this application. *See* Appeal Br. 14–16 (Claims App.); Final Act. 1. We have jurisdiction over the pending claims under 35 U.S.C. § 6(b).

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[1] We use the word "Appellant" to refer to "Applicants" as defined in 37 C.F.R. § 1.42(a). The Appeal Brief identifies NXP USA, Inc., as the real party in interest. Appeal Br. 3.

We REVERSE.

INVENTION

The invention is directed to a "packet processing architecture." *See* Abstract. Claims 1 and 10 are independent. Claim 1 is illustrative of the invention and is reproduced below.

> 1. A packet processing architecture comprising a plurality of packet processing stages arranged in series to form a pipeline for processing packets, wherein at least one of the packet processing stages comprises multiple next processing stage modules that are operably coupled to respective further packet processing stages,
>
> wherein the at least one of the packet processing stages comprises a first next processing stage register and a second next processing stage register, the first next processing stage register and the second next processing stage register connected to different packet processing stages of the plurality of packet processing stages,
>
> and wherein the at least one of the packet processing stages dynamically evaluates which one of the first and second next processing stage registers should be utilised by processing a received data packet to determine content of the received data packet and performing a stateful examination of the content, and selects one of the first and second next processing stage registers for utilization based on the processing.

PRIOR ART

Name	Reference	Date
Favor	US 7,512,129 B1	Mar. 31, 2009
Fischer	US 2007/0183415 A1	Aug. 9, 2007

REJECTION AT ISSUE[2]

Claims 1, 3, 4, 7–12, and 14–16 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Fischer and Favor. Final Act. 2–5.

ANALYSIS

We have reviewed Appellant's arguments in the Briefs, the Examiner's rejection, and the Examiner's response to Appellant's arguments. Appellant's arguments have persuaded us of error.

CLAIMS 1, 3, 4, 7–12, AND 14–16: OBVIOUSNESS OVER FISCHER AND FAVOR

Pipeline

Independent Claim 1 recites, *inter alia*, "[a] packet processing architecture comprising a plurality of packet processing stages arranged in series to form a pipeline for processing packets." Independent Claim 10 contains commensurate recitations.

The Examiner finds, *inter alia*, "Fischer differs from the claim, in that, it does not specifically disclose to form a pipeline." Final Act. 3. The Examiner further finds:

> Favor, for example, from the similar field of endeavor, teaches mechanisms to form a pipeline (see fig. 5 or fig. 3); which would have been obvious before the effective filing date of the claimed invention to and can be easily adopted by a person having ordinary skill in the art to incorporate Favor into the system of Fischer.

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[2] Throughout this Decision, we refer to the Appeal Brief ("Appeal Br.") filed October 4, 2018, the Reply Brief ("Reply Br.") filed January 28, 2019, the Final Office Action ("Final Act.") mailed March 22, 2018, the Examiner's Answer mailed November 26, 2018, and the Specification ("Spec.") filed June 24, 2015.

Id. at 3–4.

Appellant contends Favor fails to disclose the term "pipeline." Appellant argues the referenced figures disclose, respectively "SWITCHING UNIT 500" and "SWITCHING UNIT 300," but there is no disclosure that any portion thereof forms a pipeline, as claimed. Appeal Br. 12.

The Examiner finds: "the term 'pipeline' does not appear to carry specific meaning in the claim body, nor is it clearly defined to have a specific meaning or function. Hence, the term 'pipeline', which is known in the art, is being interpreted as 'plurality of functional components in serial layout.'" Ans. 11–12 (citing the generalist Oxford online dictionary). The Examiner further finds:

> [T]he examiner did not interpret that the functional components of Fischer's fig. 5 are in pipeline layout although a skilled artisan may have interpreted that fig. 2 of Fischer being a pipeline layout. Nonetheless, Favor (or even Fischer) indeed teaches or suggests "… a plurality of packet processing stages arranged in series to form a pipeline for processing packets …", as recited in claim 1.

Ans. 12.

Appellant contends the Examiner's Answer departs from the definition for "pipeline" adopted by the Examiner ("A linear sequence of specialized modules used for pipelining"). Reply Br. 6–7. Appellant argues where the Examiner relies on the cited dictionary definition to interpret the term "pipeline," the Examiner has to show the teachings of the relied-upon references disclose not only "a linear sequence of specialized modules," but also disclose "used for pipelining," which, Appellant contends, the Examiner has not done. Reply Br. 7.

We agree with Appellant. The Examiner finds "the term 'pipeline', which is known in the art, is being interpreted as 'plurality of functional components in serial layout.'" Ans. 11–12 (citing the Oxford Online Dictionary). We do not adopt the Examiner's claim construction because it fails to reference the Specification. "Even under the broadest reasonable interpretation, the Board's construction cannot be divorced from the specification and the record evidence." *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) (internal quotes and citation omitted). The MPEP makes clear that the intrinsic record (e.g., the specification) must be consulted to identify which of the different possible definitions is most consistent with the invention's use of the terms. *See* MPEP § 2111.01 (III) quoting *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1300 (Fed. Cir. 2003) ("Where there are several common meanings for a claim term, the patent disclosure serves to point away from the improper meanings and toward the proper meanings.").

The Examiner finds "the term 'pipeline' does not appear to carry specific meaning in the claim body, nor is it clearly defined to have a specific meaning or function." Ans. 11. Appellant discloses:

> In a computing context, a pipeline is a set of packet processing elements connected in series, so that the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in a time-sliced fashion.

Spec., 1. Appellant further discloses:

> At the end of its operation, a number of frame manager stages 102-116 may dispatch a user-programmable next processing stage (NPS) code, which may be used by the frame manager module's hardware to determine the next stage in the processing pipeline. In this way, the frame manager module

> 100 may allow a user to configure the pipeline stages 102-116, thereby allowing each application to perform different functions on the received data packets.

Spec., 2. The Examiner fails to acknowledge Appellant's disclosure regarding the claimed "pipeline." The Examiner fails to provide a reason why Appellant's disclosure fails to define the claimed term even by implication. "Even when guidance is not provided in explicit definitional format, the specification may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents." *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1150 (Fed. Cir. 2012) (quoting *Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004)).

The Examiner finds "Favor either in fig. 5 or fig. 3 discloses such pipeline layout comprising 'Incoming Buffer -Primary Processing Unit - Secondary Unit - Outgoing Buffer' in serial layout for processing packets." Ans. 12.

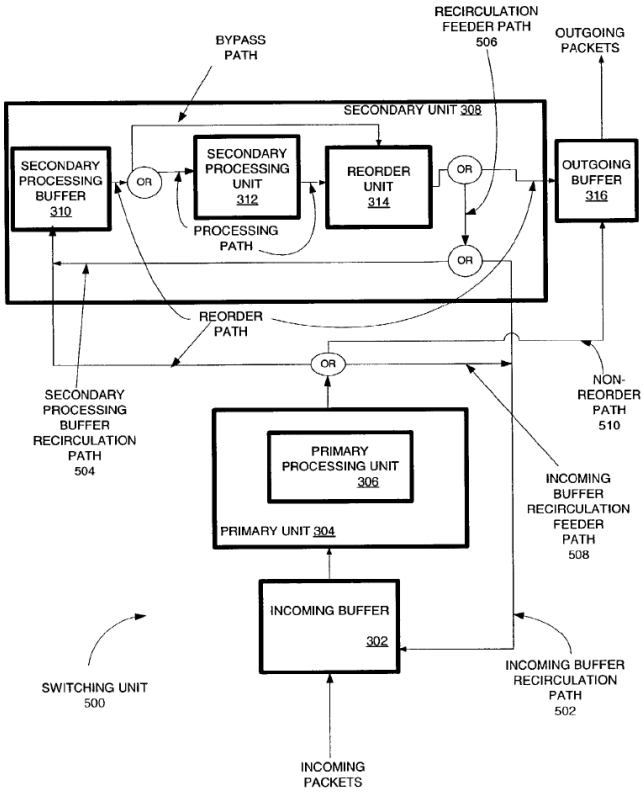

FIG. 5

Favor, Figure 5 showing a packet may be processed by a variety of paths including reorder, nonreorder, and various recirculation paths.

Contrary to the Examiner, Favor Figure 5, discloses a packet is not confined to a serial path, but may be processed by a variety of non-linear paths. We find the Examiner cited portions of the prior art fail to teach or suggest "[a] packet processing architecture comprising a plurality of packet processing stages arranged in series to form a pipeline for processing packets," as recited in independent Claims 1 and 10.

In view of the foregoing, we decline to sustain the rejection of Claims 1, 3, 4, 7–12, and 14–16 under 35 U.S.C. § 103.

CONCLUSION

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 3, 4, 7–12, 14–16	103	Fischer, Favor	--	1, 3, 4, 7–12, 14–16

REVERSED