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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEVEN J. WALLACH and TONY M. BREWER

Appeal 2019-002211
Application 15/596,649
Technology Center 2100

Before BARBARA A. BENOIT, IRVIN E. BRANCH, and MICHAEL J. ENGLE, *Administrative Patent Judges.*

ENGLE, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–20, which are all of the claims pending in the application.[1] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Micron Technology, Inc. as the real party in interest. Appeal Br. 2.

TECHNOLOGY

The application relates to a computing system with "two memory access paths: 1) a cache-access path in which block data is fetched from main memory for loading to a cache, and 2) a direct-access path in which individually-addressed data is fetched from main memory." Spec. Abstract.

ILLUSTRATIVE CLAIM

Claim 1 is illustrative and reproduced below with certain limitations at issue emphasized:

> 1. A memory system providing memory access for a multiple processor system including at least one processor and at least one heterogeneous functional unit, the at least one processor configured to execute at least one instruction of a first instruction set and the at least one heterogeneous functional unit configured to execute at least one instruction of a second instruction set that is different than the first instruction set, the memory system comprising:
>
> *a main memory configured for individually-addressed data access*;
>
> a block oriented cache-access path coupling the main memory and a cache memory, wherein the block oriented cache-access path is configured to provide fixed-size data block access to the main memory, and wherein the cache memory provides storage of fixed-size data blocks of main memory data for data access by the at least one processor; and
>
> an address oriented cache-bypass path coupling the main memory and the at least one heterogeneous functional unit, wherein *the address oriented cache-bypass path provides individually-addressed data access to the main memory*.

REFERENCES

The Examiner relies on the following prior art references:

Name	Patent Number	Date
Castelli	US 2002/0099907 A1	July 25, 2002
Fossum	US 4,888,679	Dec. 19, 1989
Sheaffer	US 2004/0236920 A1	Nov. 25, 2004
Van Doren	US 2004/0068622 A1	Apr. 8, 2004
Wallach	US 9,710,384 B2	July 18, 2017

REJECTIONS

The Examiner made the following rejections:

Claims	Basis	Reference(s)
1, 4, 8, 9, 15, 17	Double patenting	Wallach, Castelli
1–3, 5, 8–12, 15–18	§ 102	Fossum
4	§ 103	Fossum, Sheaffer
6, 7, 13, 14, 19, 20	§ 103	Fossum, Van Doren

ISSUE

Did the Examiner err in finding Fossum discloses "a main memory configured for individually-addressed data access" and "the address oriented cache-bypass path provides individually-addressed data access to the main memory," as recited in claim 1?

ANALYSIS

Double Patenting

Appellant does not substantively dispute the double patenting rejection and instead states that "Appellant has proposed that if, at the time the claims of the present application are determined to include allowable subject matter, a double patenting rejection is proper, a terminal disclaimer will be filed at that time." Appeal Br. 4. The Examiner notes that "Appellant has not filed a Terminal Disclaimer as [of] the writing of this

Examiner's Answer, thus claims 1, 4, 8, 9, 15 and 17 remain rejected in view of double patenting." Ans. 3.

Accordingly, we affirm the Examiner's double patenting rejection.

§ 102

Independent claims 1 and 17 recite "a main memory configured for *individually-addressed* data access" and "the address oriented cache-bypass path provides *individually-addressed* data access to the main memory." Independent claim 9 similarly recites "providing *individually-addressed* data access to the main memory . . . via an address oriented cache-bypass path."

Appellant argues that in Fossum, access to main memory is always a *block* access, not an "individually-addressed" access as required by the claims. Appeal Br. 6.

The Examiner finds that Fossum discloses "individually-addressed" in three ways. First, the Examiner determines that the claims do not limit the size of the "block" and therefore the claimed block could be "simply only one data element." Ans. 6–7. Even if we were to agree with that broad interpretation, Appellant is correct that "[n]othing in *Fossum* suggests that a block of data can have a size of 1" and instead "the only examples given in *Fossum* propose a data block size of 64 bytes." Appeal Br. 4; Fossum 5:59 ("The block size, for example, is 64 bytes."), 11:30–32. This is an anticipation rejection, not obviousness, yet Fossum alone does not disclose an "individually-addressed" "block" of size 1.

Second, the Examiner finds that in addition to Fossum disclosing block-access by a vector processing unit, Fossum also discloses that an individual data unit can be sent to a *scalar* processing unit. *E.g.*, Ans. 8–9. A "scalar processing unit . . . receives and operates on only one single data

element at a time." *Id.* at 12. "[T]hus while a fixed-size block data may be received from the main memory and stored in the cache memory's data store, only the single data element requested by the scalar processing unit is delivered to, and received by, the scalar processing unit." *Id.* (emphasis and citation omitted). Even setting aside the issue of whether the Examiner is treating Fossum's scalar processing unit as the claimed "processor" for some limitations versus the claimed "heterogeneous functional unit" for others, *see* Reply Br. 5, we agree with Appellant that claim 1 requires "a *main memory* configured for individually-addressed data access." Here, the Examiner agrees that the main memory access is by block, not individually-addressed. Ans. 12; Fossum 4:36–41 ("If a data element needed by the *scalar* processor is not found in the cache 24, then the data element is obtained from the main memory 23, but in the process *an entire block, including additional data, is obtained from the main memory* 23 and written into the cache 24." (emphasis added)). Therefore, Fossum's scalar processing unit fails to disclose the limitation as claimed.

Third, the Examiner finds that when accessing a vector, the vector processor first calculates each individual address within that vector. Ans. 9–10. But Appellant correctly points out that the individual addresses are never sent to the memory; instead, the individual addresses are only used to determine which *blocks* are needed from memory, then only the *blocks* are requested from memory. *See* Reply Br. 5–6; Fossum 7:37-43 ("The logic circuit 40 determines the *blocks* of data which include at least one data element of a given vector by sequentially computing the addresses associated with each of the successive data elements of the vector, and

testing whether each computed address is within a different block from the previously computed address." (emphasis added)).

We therefore agree with Appellant that Fossum fails to disclose a main memory configured for individually-addressed data access.

Accordingly, we do not sustain the Examiner's § 102 rejection of independent claims 1, 9, and 17, and their dependent claims 4, 8, and 15.

§ 103

The Examiner does not rely on the additional references Sheaffer or Van Doren to cure the deficiencies of Fossum. Accordingly, we reverse the Examiner's § 103 rejections of dependent claims 4, 6, 7, 13, 14, 19, and 20.

DECISION

The following table summarizes the outcome of each rejection:

Claims Rejected	Statute	Basis	Affirmed	Reversed
1, 4, 8, 9, 15, 17		Obviousness-type double patenting	1, 4, 8, 9, 15, 17	
1–3, 5, 8–12, 15–18	§ 102	Fossum		1–3, 5, 8–12, 15–18
4	§ 103	Fossum, Sheaffer		4
6, 7, 13, 14, 19, 20	§ 103	Fossum, Van Doren		6, 7, 13, 14, 19, 20
OVERALL			1, 4, 8, 9, 15, 17	2, 3, 5–7, 10–14, 16, 18–20

TIME TO RESPOND

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.36(a)(1)(iv).

AFFIRMED-IN-PART