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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/881,477	10/13/2015	Martin Poelzl	1012-1677 / 2014P51178 US	8689
57579	7590	08/28/2020	EXAMINER	
MURPHY, BILAK & HOMILLER/INFINEON TECHNOLOGIES 1255 CRESCENT GREEN SUITE 200 CARY, NC 27518			GEBREMARIAM, SAMUEL A	
			ART UNIT	PAPER NUMBER
			2811	
			NOTIFICATION DATE	DELIVERY MODE
			08/28/2020	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MARTIN POELZL, OLIVER BLANK, FRANZ HIRLER,
MAXIMILIAN ROESCH, and LI JUIN YIP

Appeal 2019-002146
Application 14/881,477
Technology Center 2800

Before BEVERLY A. FRANKLIN, N. WHITNEY WILSON, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

WILSON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant¹ appeals under 35 U.S.C. § 134(a) from the Examiner's
December 15, 2017 decision finally rejecting claims 1–14 (“Final Act.”).²
We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We reverse.

¹ We use the word “Appellant” to refer to “applicant” as defined in
37 C.F.R. § 1.42. Appellant identifies INFINEON TECHNOLOGIES
AUSTRIA AG, as the real party in interest (Appeal Br. 2).

² Claims 15–20 have been withdrawn from consideration and are not on
appeal (Final Act. 1).

CLAIMED SUBJECT MATTER

Appellant's invention is directed to method of manufacturing a semiconductor device (Spec. 3). The claimed method includes forming first trenches extending from a process surface into a semiconductor layer (*id.*). An alignment layer with mask pits in a vertical projection of the first trenches is formed on the process surface (*id.*). A gate trench for a gate structure is formed in a mesa section between the first trenches, wherein the auxiliary material is used as an etch mask. (*Id.*). Details of the claimed invention are described in claim 1, which is reproduced below from the Claims Appendix of the Appeal Brief:

1. A method of manufacturing a semiconductor device, the method comprising:
 - forming first trenches extending from a process surface into a semiconductor layer;
 - forming, on the process surface, an alignment layer comprising mask pits formed in the alignment layer in a vertical projection of the first trenches, wherein sidewalls of the mask pits have a smaller tilt angle with respect to the process surface than sidewalls of the first trenches;
 - filling the mask pits with an auxiliary material; and
 - forming, by using the auxiliary material as an etch mask, a gate trench for a gate structure in a mesa section of the semiconductor layer between the first trenches.

REJECTIONS

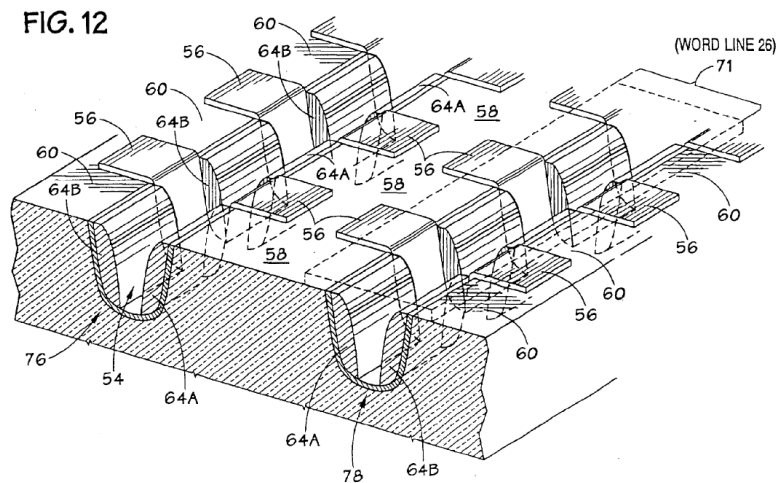
1. Claims 1–5 and 10–14 are rejected under 35 U.S.C. § 102(a)(2) as anticipated by Gonzalez.³
2. Claims 6–9 are rejected under 35 U.S.C. § 103 as unpatentable over Gonzalez.

³ Gonzalez, US 6,798,013 B2, issued September 28, 2004.

DISCUSSION

“A prior art reference anticipates a patent claim under 35 U.S.C. § 102(b) if it discloses every claim limitation.” *In re Montgomery*, 677 F.3d 1375, 1379 (Fed. Cir. 2012) (citing *Verizon Servs. Corp. v. Cox Fibernet Va., Inc.*, 602 F.3d 1325, 1336–37 (Fed. Cir. 2010)). In this instance, Appellant contends that Gonzalez does not teach “forming, by using the auxiliary material as an etch mask, a gate trench for a gate structure in a mesa section of the semiconductor layer between the first trenches” (Appeal Br. 3) (emphasis omitted).

The Examiner finds that this limitation is taught by Gonzalez as illustrated in Gonzalez’s FIG. 12:



Gonzalez’s FIG. 12 shows a step in constructing a multi-bit memory cell.

The Examiner finds that:

Gonzalez clearly teaches that fig. 12 is a partial cross-section view of a number of transistors 10 formed by the above process. ***Referring to the rows (76 and 78) for example, one can clearly see three trenches, where between the two trenches on the opposite ends of figure 12, a gate trench is formed in the mesa section (58) between the opposite ends of the first trenches . . .***

... one clearly sees three trenches where between the two trenches on the opposite ends of figure 12, a gate trench (in the middle of the rows 76/78) is formed in the mesa section (58) between the opposite ends of the first trenches

Ans. 2–3 (emphasis added). However, in looking at FIG. 12, there is no trench shown in the mesa section 58 between rows 76 and 78. Thus, the evidence of record simply does not support the Examiner’s finding that there is a gate trench formed in the mesa section 58 between the two trenches.

To the extent that the Examiner’s anticipation rejection is based on an inartfully explained finding that there is a third trench that is not shown in the FIG. 12, and one of the trenches (either 76 or 78) corresponds to the claimed gate trench, claim 1 recites that the gate trench is formed by using auxiliary material as an etch mask. However, the material identified by the Examiner as corresponding the claimed auxiliary layer (layer 66) is applied after the trenches 54 have been etched into the substrate (compare Gonzalez FIG. 7 to Gonzalez FIG. 9) and, therefore, cannot be used to as an etch mask in preparing trench 54.

Accordingly, we determine that Appellant has shown reversible error in the anticipation rejections. Because this erroneous finding is also central to the obviousness rejection of dependent claims 6–9, we reverse that rejection as well.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1-5, 10-14	102(a)(2)	Gonzalez		1-5, 10-14
6-9	103	Gonzalez		6-9
Overall Outcome				1-14

REVERSED