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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/158,483	01/17/2014	Chih-Chien Chi	TSM13-1198	5673

43859 7590 01/28/2020

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EXAMINER	
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ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
01/28/2020	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CHIH-CHIEN CHI, HUANG-YI HUANG, SZU-PING TUNG, and CHING-HUA HSIEH

Appeal 2019-001993
Application 14/158,483
Technology Center 2800

Before DONNA M. PRAISS, MICHELLE N. ANKENBRAND, and CHRISTOPHER L. OGDEN, *Administrative Patent Judges.*

PRAISS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

Appellant[2] appeals under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 10, 12, 21–25, 30–34, and 37–44. We have jurisdiction over the appeal under 35 U.S.C. § 6(b).

We AFFIRM.

[1] Our Decision refers to the Specification ("Spec.") filed Jan. 17, 2014, the Final Office Action ("Final Act.") dated Oct. 24, 2017, Appellant's Appeal Brief ("Appeal Br.") filed May 30, 2018, the Examiner's Answer ("Ans.") dated Nov. 7, 2018, and Appellant's Reply Brief ("Reply Br.") filed Jan. 7, 2019.

[2] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies Taiwan Semiconductor Manufacturing Company LTD. as the real party in interest. Appeal Br. 2.

STATEMENT OF THE CASE

The invention relates to methods for forming an interconnect structure electrically coupled to semiconductor devices and other electrical devices to form an electrical circuit. Spec. ¶ 1. According to the Specification, the layers of conductive lines separated by layers of dielectric material in the interconnect structure extend substantially parallel to the semiconductor substrate and may include metal patterns of vertically spaced metallization layers electrically interconnected by vias. *Id.*

Claims 10, 25, and 31, the independent claims on appeal reproduced below from the Claims Appendix to the Appeal Brief, are illustrative (disputed limitations italicized).

> 10. A method for forming an interconnect structure, the method comprising:
>
> forming a trench in a first dielectric layer;
>
> filling the trench with a conductive material;
>
> planarizing a surface of the conductive material and a surface of the first dielectric layer;
>
> removing impurities from the surface of the conductive material, the removing comprising using a first thermal process in a first vacuum ambient or a first inert gas ambient, wherein the first inert gas ambient is an Ar gas ambient, a He gas ambient, or a combination thereof;
>
> *forming a capping layer over and in physical contact with the conductive material and all other conductive lines within the first dielectric layer after the removing the impurities*, wherein the forming the capping layer further comprises:
>
> blanket depositing a first material onto the first dielectric layer and the conductive material; and
>
> etching the first material to remove portions of the first material located on a top surface of the first dielectric layer;

removing impurities from the surface of the capping layer, the removing impurities from the surface of the capping layer comprising using a second thermal process in a second vacuum ambient or a second inert gas ambient, wherein the second inert gas ambient is an Ar gas ambient, a He gas ambient, or a combination thereof;

forming a second dielectric layer over and directly adjoining the surface of the first dielectric layer and over and directly adjoining the surface of the capping layer, wherein at the time of the forming the second dielectric layer the capping layer comprises a single material with a single composition throughout the capping layer; and

forming a metallization layer over the second dielectric layer, *wherein after the forming the metallization layer the capping layer consists essentially of CoP, CoB, Co WP, CoWB, NiWP, CoSnP, NiWB, or NiMoP*.

25. A method for forming an interconnect structure, the method comprising:

providing a workpiece, the workpiece having a first dielectric layer and a conductive feature formed in the first dielectric layer, a top surface of the first dielectric layer and a top surface of the conductive feature being co-planar;

removing impurities by exposing the top surface of the first dielectric layer and the top surface of the conductive feature to a first thermal process in an ambient of a first vacuum without gas, wherein the first thermal process is performed at a temperature of between 400 °C and 500 °C for a time of between about 5 minutes and about 30 minutes;

after the removing, forming a capping layer from a single material over and directly adjoining the top surface of the conductive feature;

after the forming the capping layer, removing impurities from the capping layer, wherein the removing impurities from the capping layer comprises using a second thermal process in a second vacuum without gas, wherein the second thermal

process is performed at a temperature of between 400 °C and 500 °C for a time of between about 5 minutes and about 30 minutes;

after the forming the capping layer, forming a second dielectric layer over and directly adjoining the top surface of the capping layer, wherein after the forming the second dielectric layer the surface of the capping layer into physical contact with the second dielectric layer consists essentially of CoP, CoB, Co WP, CoWB, NiWP, CoSnP, NiWB, or NiMoP; and

after the forming the second dielectric layer, *permanently electrically connecting the conductive feature to a metallization layer*.

31. A method for forming an interconnect structure, the method comprising:

providing a workpiece having a copper line in a first dielectric layer, the top surface of the copper line and a top surface of the first dielectric layer being substantially co-planar;

removing impurities from a top surface of the copper line and the top surface of the first dielectric layer, the removing comprising using a first thermal process and at least one of a first ambient of a first vacuum or a first inert gas, wherein the first inert gas is an Ar gas, a He gas, or a combination thereof, wherein the first thermal process is performed at a temperature of between 400 °C and 500 °C for a time of between about 5 minutes and about 30 minutes;

selectively plating a capping layer in physical contact with the top surface of the copper line after the removing the impurities from the top surface of the copper line, wherein the capping layer is conductive, wherein the capping layer has a top surface facing away from the copper line at the end of the selectively plating the capping layer, *wherein the selectively plating the capping layer comprises placing a plating solution into contact with each conductive line exposed within the first dielectric layer*;

removing impurities from the top surface of the capping layer after the selectively plating capping layer and while the

top surface of the capping layer is exposed, wherein the removing impurities from the top surface of the capping layer comprises using a second thermal process and at least one of a second ambient of a second vacuum or a second inert gas, wherein the second inert gas is an Ar gas, a He gas, or a combination thereof, wherein the second thermal process is performed at a temperature of between 400 °C and 500 °C for a time of between about 5 minutes and about 30 minutes and at a pressure of about 10^{-6} mTorr, the capping layer comprising a single material with a single composition throughout the capping layer after the removing the impurities; and

forming an overlying layer over the first dielectric layer, wherein the overlying layer is in direct physical contact with the top surface of the capping layer.

The References

The Final Office Action cites the following prior art references.

Name	Reference	Date
Braeckelmann	US 6,218,302 B1	Apr. 17, 2001
Ballantine	US 6,339,022 B1	Jan. 15, 2002
Lopatin	US 2005/0101130 A1	May 12, 2005
Yun	US 2007/0059912 A1	Mar. 15, 2007
Yu	US 2007/0228571 A1	Oct. 4, 2007
Bei	US 2012/0070915 A1	Mar. 22, 2012
Bao	US 2014/0021578 A1	Jan. 23, 2014

The Rejections

The Examiner maintains the following rejections. Ans. 2.[3]

Claim(s)	35 U.S.C. §	Basis/Reference(s)
10, 12, 21–24, 37–44	112(a)	Written description
31–34	112(a)	Written description
10, 12, 21–24, 37–44	103	Bao, Yu, Ballantine, Braeckelmann, Lopatin
25, 30	103	Bao, Braeckelmann, Ballantine
31–34	103	Bao, Ballantine, Bei, Yun

ANALYSIS

We review the appealed rejections for error based upon the issues Appellant identifies. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (*cited with approval in In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("[I]t has long been the Board's practice to require an applicant to identify the alleged error in the examiner's rejections.")). After considering the positions of both the Examiner and Appellant, we find the Examiner reversibly erred in rejecting the claims under 35 U.S.C. § 112(a), however,

[3] The Examiner provided an initial Answer dated Oct. 4, 2018, and a subsequent Answer dated Nov. 7, 2018. All citations herein are to the subsequent Answer dated Nov. 7, 2018, because it is inclusive of the Examiner's earlier response and additionally responds to Appellant's arguments concerning the Section 103 rejections.

we are not persuaded of harmful error in the Examiner's rejections under 35 U.S.C. § 103 for the reasons discussed below.

Rejection 1: Written Description (Claim 10 and Dependents)

The Examiner rejects claim 10 and its dependent claims 12, 21–24, and 37–44 under 35 U.S.C. § 112(a) for failing to disclose in the Specification the recited "forming a capping layer over and in physical contact with the conductive material and all conductive lines within the first dielectric layer." Final Act. 3–4. According to the Examiner, the Specification only discloses forming a capping layer over and in physical contact with the conductive material, not "all other conductive lines" within the first dielectric layer as claimed. *Id.* at 4. The Examiner also finds the Specification does not specify that the capping layer composition is unchanged after further processing. *Id.*

As to the capping layer composition, Appellant contends "while Appellant's Specification does describe[] further process steps after the capping layer has been formed . . . , these processes do not modify the materials of the capping layer," which is disclosed as consisting essentially of CoP, CoB, CoWP, CoWB, NiWP, CoSnP, NiWB, or NiMoP. Appeal Br. 11 (citing Spec. ¶¶ 20, 21). According to Appellant, removing impurities does not chemically modify the material and depositing a material over the capping layer does not transform the capping layer material into another material. *Id.* at 11–12 (citing Spec. ¶¶ 17, 23, 25). Appellant also asserts that the explicit disclosure of a dielectric layer deposition using physical vapor deposition implicitly discloses the structure after such a process, which

would be understood by one of ordinary skill in the art as not chemically modifying the underlying material. *Id.* at 14.

In response, the Examiner finds that removing impurities from the capping layer would change the capping layer composition because the capping layer comprises capping material and impurities (i.e., gas) before the process, and after removal of the impurities, the capping layer comprises capping material. *Id.* at 3. The Examiner also points to a lack of evidence that forming the metallization layer would not introduce impurities into the capping layer or that the metal of the metallization would not diffuse into the capping layer. *Id.* at 3–4.

As to forming a capping layer over and in physical contact with all other conductive lines, Appellant points to the Specification's disclosure that "the cap layer 440 may be selectively formed on the conductive line 208 and top edges of the liner 206, ***if conductive***" means that the cap layer is selectively deposited on the conductive materials, which includes conductive line 208 and liner 206. *Id.* at 17 (citing Spec. ¶ 22). Appellant asserts that interconnect lines generally include layers of conductive lines separated by layers of dielectric material in interconnect structures, the conductive lines may include metal patterns, and the metal lines formed in trench-like openings typically extend substantially parallel to the semiconductor substrate. *Id.* at 19 (citing Spec. ¶¶ 1, 2, 8). Appellant's position is that single conductive line 208 illustrated in Appellant's figures is for explanatory purposes only and would not be understood by one skilled in the art to be the only metal line within dielectric layer 104 in view of the references to multiple structures, lines, patterns within the lines, and openings. *Id.* (citing Spec. ¶ 1).

The Examiner responds that an ordinarily skilled artisan would consider a conductive line to differ from a conductive liner and that Appellant's Specification distinguishes between a conductive line and a liner. Ans. 5. The Examiner also responds that the Specification's paragraph 1 does not support the recited limitation explicitly, implicitly, or inherently because it relates to the configuration of an integrated circuit including multiple interconnect structures that is not applicable to the claimed invention. Ans. 7. According to the Examiner, a person having ordinary skill in the art would have to guess at how many conductive lines are within a dielectric layer of a multiple layer integrated circuit and how they are arranged to meet the claimed invention because the Specification lacks disclosure of a specific design of the integrated circuit. *Id.* at 8.

Appellant's arguments are persuasive of harmful error. The Specification supports the claimed "capping layer consists essentially of CoP, CoB, CoWP, CoWB, NiWP, CoSnP, NiWB, or NiMoP." *Compare* Appeal Br. 43 (Claims Appendix), *with* Spec. ¶ 21. The claim term "consisting essentially of" is used to indicate, for example, that "the invention necessarily includes the listed ingredients and is open to unlisted ingredients that do not materially affect the basic and novel properties of the invention." *PPG Indus., Inc. v. Guardian Indus. Corp.*, 156 F.3d 1351, 1354 (Fed. Cir. 1998). The Examiner's rejection of claim 10 and its dependents is based on process steps that remove impurities from the capping layer and deposit layers that may introduce impurities to the capping layer. Appellant's position is that the presence or absence of impurities in the capping layer does not change the claimed materials composing the capping layer. Appellant's position is reasonable because the Specification describes

the impurities relating to bubbling, peeling, delamination, and outgassing issues and the removal of impurities reducing and/or preventing these issues. Spec. ¶ 27; Ans. 3. Thus, the presence or absence of impurities may affect the degree to which bubbling, peeling, delamination, and outgassing may occur, but the evidence cited in this appeal record does not suggest that the degree of impurities present in the capping layer materially affects the basic and novel properties of the capping layer.

Regarding the recited conductive lines, the Examiner's rejection fails to sufficiently explain why one skilled in the art would not recognize from the Specification's disclosure (Spec. ¶ 22) of selectively forming cap layer 440 on conductive line 208 depicted in Appellant's Figures 4 and 5, as well as other exposed elements "if conductive" (e.g., liner 206) that the inventors were in possession of forming the cap layer on all conductive lines exposed. The claimed subject matter need not be described "in haec verba" in the original specification in order to satisfy the written description requirement. *In re Wright*, 866 F.2d 422, 425 (Fed. Cir. 1989). Rather, "the test . . . is whether a person of ordinary skill in the art would recognize that the applicant possessed what is claimed in the later filed application as of the filing date of the earlier filed application." *Noelle v. Lederman*, 355 F.3d 1343, 1348 (Fed. Cir. 2004). The Examiner's distinction between a line and a liner (Ans. 5) does not address the conductive property of the element the capping layer covers that the Specification highlights. Moreover, Appellant's Figure 5 shows the capping layer is formed over and in physical contact with a conductive line, which is all of the conductive lines in Figure 5.

In view of the above, we reverse the Examiner's rejection of claim 10 and its dependents as lacking written description support in the Specification.

Rejection 2: Written Description (Claim 31 and Dependents)

The Examiner rejects claim 31 and its dependent claims 32–34 under 35 U.S.C. § 112(a) on the basis that the limitation "wherein the selectively plating the capping layer comprises placing a plating solution into contact with each conductive line exposed within the first dielectric layer" is not disclosed in the Specification. Final Act. 4–5. Specifically, the Examiner finds that the Specification discloses forming a capping layer over and in physical contact with "a conductive line" and does not disclose "other conductive lines." *Id.* at 4.

Appellant contends the Examiner's rejection of claim 31 is in error in view of the Specification's paragraph 22 disclosure quoted above in connection with the similar rejection of claim 10. Appeal Br. 28. Appellant also cites Specification paragraphs 1 and 8 for disclosing multiple lines such that a person having ordinary skill in the art would understand that conductive line 208 in Appellant's figures is representative of multiple lines present. Appeal Br. 29–30. Appellant argues that it would neither be rational nor technically possible for a skilled artisan, upon reading the Specification, to understand that the integrated circuit comprises only a single conductive line in a single dielectric layer. *Id.* at 30.

The Examiner relies on the same response provided with respect to the rejection of claim 10. Ans. 9.

Because Appellant's argument that the Examiner erred in rejecting claim 10 under 35 U.S.C. § 112(a) is persuasive of harmful error for the reasons discussed above, we likewise reverse the Examiner's rejection of claim 31 and its dependents as lacking written description support in the Specification.

Rejection 3: Obviousness of Claims 10, 12, 21–24, and 37–44

The Examiner rejects claims 10, 12, 21–24, and 37–44 under 35 U.S.C. § 103 as being unpatentable over Bao in view of Yu, Ballantine, Braeckelmann, and Lopatin. Final Act. 6–12. Claims 12, 21–24, and 37–44 depend directly or indirectly from claim 10. Appellant argues only claim 10, which we select as representative.

Appellant contends the Examiner's rejection is in error because Bao's conductive cap 414 is only formed on Bao's second M_x metal 410 and not over Bao's first M_x metal 408 as depicted in Bao's Figure 4C. Appeal Br. 34–35. Bao's Figure 4C is shown below.

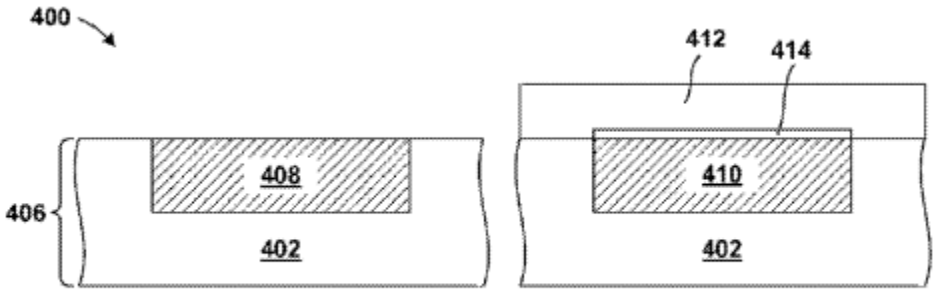

FIG. 4C

Figure 4C above depicts an embodiment where mask 412 is applied on top of conductive cap 414 above second M_x metal 410 and a portion the conductive cap from above first M_x metal 408 is removed. Bao ¶¶ 31, 70. Appellant asserts Bao teaches the capping layer is only to be used on e-

fuses, not on the remaining structures, and quotes Bao stating "[i]t should be noted that neither the first M_x metal 408 nor the M_{x+1} metal 422 have a conductive cap." Appeal Br. 35 (quoting Bao ¶ 75).

The Examiner responds that the embodiment depicted in Bao's Figure 4B, not 4C, is relied upon for the rejection, and that Figure 4B depicts conductive cap 414 over both first M_x metal 408 and second M_x metal 410. Ans. 10 (citing Bao Fig. 4B). Bao's Figure 4B is reproduced below.

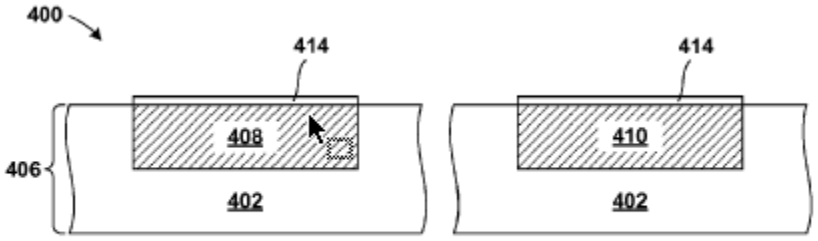

FIG. 4B

Figure 4B above depicts the deposition of a conductive cap above the first and second M_x metals according to an embodiment. Bao ¶ 30. The Examiner notes that claim 10 does not exclude any processing steps performed on other conductive lines after the capping layer is formed. Ans. 10.

In the Reply Brief, Appellant requests that we consider Bao in its entirety and not merely the portions upon which the Examiner relies. Reply Br. 13.

The preponderance of the evidence cited in this Appeal record supports the Examiner's rejection of claim 10. As the Examiner notes, claim 10 does not preclude additional steps from being performed on the capping layer after it is formed. Therefore, the Examiner's reliance on particular disclosures in Bao is appropriate. In a determination of obviousness, a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art. *Merck & Co. v. Biocraft Labs.*, 874

F.2d 804, 807 (Fed. Cir. 1989) ("That the [prior art] patent discloses a multitude of effective combinations does not render any particular formulation less obvious."). Moreover, "a reference is not limited to the disclosure of specific working examples." *In re Mills*, 470 F.2d 649, 651 (CCPA 1972) (citation omitted).

Accordingly, we sustain the Examiner's rejection of claims 10, 12, 21–24, and 37–44 under § 103.

Rejection 4: Obviousness of Claims 25 and 30

The Examiner rejects claims 25 and 30 under 35 U.S.C. § 103 as being unpatentable over Bao in view of Braeckelmann and Ballantine. Final Act. 12–15. Claim 30 depends from claim 25. Appeal Br. 44 (Claims Appendix). Appellant argues only claim 25, which we select as representative.

Appellant contends the Examiner erred because the presence of void 428 in Bao's final vertical e-fuse structure fails to disclose "permanently electrically connecting the conductive feature to a metallization layer" as recited in claim 25. Appeal Br. 37 (citing Bao Fig. 4F). Bao's Figure 4F is shown below.

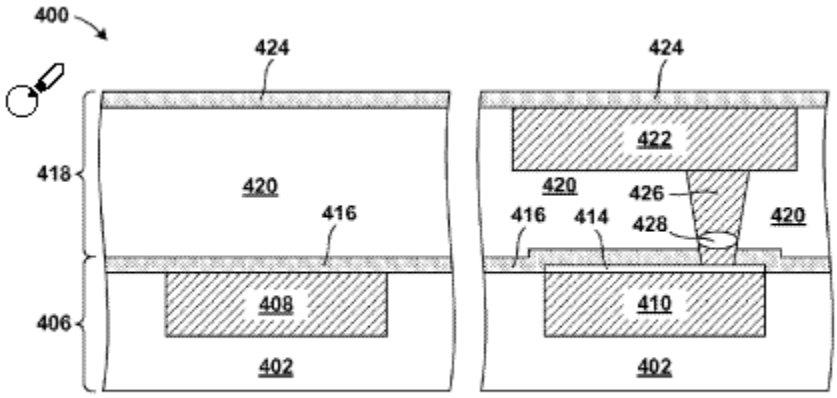

FIG. 4F

Figure 4F above depicts Bao's final vertical e-fuse structure after programming. Bao ¶¶ 34, 76. Appellant argues that a person of ordinary skill in the art would not have had a reason to modify Bao to prevent the formation of void 428 because the entire purpose of Bao's conductive cap 314 is to "encourage the formation of a void." Appeal Br. 38 (quoting Bao ¶ 52).

The Examiner responds that Bao's Figure 4F is not relied upon in the rejection because Figure 4F refers to the final vertical e-fuse structure after programming and the claim does not require the step of programming the interconnect structure. *Id.* at 11–12. Regarding Bao's disclosure of forming voids, the Examiner responds that the purpose of Bao's conductive cap 314 is to improve electromigration resistance between the second M_x metal and the via and to help prevent the migration of the conductive interconnect material from the second M_x metal to the via to prevent voids from forming, as shown in Bao's Fig. 1. *Id.* at 12 (citing Bao ¶ 76).

In the Reply Brief, Appellant notes that the Examiner erroneously characterizes claim 25 as a device claim when the claim instead recites a method. Reply Br. 14. Appellant agrees with the Examiner that claim 25

does not require programming, but contends that "claim 25 does require '**permanently** electrically connecting the conductive feature to a metallization layer,'" which "the Examiner has not yet illustrated is disclosed or rendered obvious by the cited references." *Id.* at 16. Appellant also asserts that Bao does not disclose such a permanent electrical connection because "Bao specifically describes an 'open circuit' to electrically disconnect the structures within Bao." *Id.* (citing Bao ¶ 76, Fig. 4F).

Appellant correctly points out that claim 25 is directed to a method and not a device as the Examiner states; however, we do not find this to be harmful error. The Examiner finds that Bao discloses that the void only is intentionally generated under a specified condition with a specific current to a specific targeted structure. Ans. 11 (citing Bao ¶¶ 4, 8). Appellant does not dispute this finding, which the record supports. Bao ¶¶ 4, 8. The Examiner also determines that claim 25 does not require programming the interconnect structure, which programming step in Bao refers to intentionally blowing a fuse and creating an open circuit. Ans. 11; Bao ¶ 4. As noted above, Appellant agrees with the Examiner's determination. Therefore, Bao's Figure 4F is not part of the rejection. Ans. 11–12. Accordingly, the preponderance of the evidence supports the Examiner's determination that the claimed method would have been obvious in view of the cited prior art references prior to any programming step. Therefore, we sustain the Examiner's rejection of claims 25 and 30 under § 103.

Rejection 5: Obviousness of Claims 31–34

The Examiner rejects claims 31–34 under 35 U.S.C. § 103 as being unpatentable over Bao in view of Ballantine, Bei, and Yun. Final Act. 15–19.

Appellant contends the Examiner erred because the Examiner has not shown that Bao's plating technique inherently comprises placing a plating solution into contact with each conductive line exposed within the first dielectric layer as claim 31 recites. Appeal Br. 39; Final Act. 15 (citing Bao ¶ 69 and referring explicitly to exposed surfaces of M_x metals 408 and 410 in Bao). Appellant asserts that because Bao depicts only two M_x metals, but discloses that more than two M_x metals may be included on a single chip, putting each of Bao's M_x metals into contact with a plating solution is not necessarily present. Appeal Br. 39–40. According to Appellant, because Bao's structure may be partially inserted into a plating solution to plate Bao's first and second M_x metals without plating the rest, Bao's process would not result in "selectively plating the capping layer compris[ing] placing a plating solution into contact with each conductive line exposed within the first dielectric layer" as required by claim 31. *Id.*

The Examiner responds that the same reasons stated with respect to claim 10 also apply to the rejection of claim 31 and its dependents. Ans. 12.

In the Reply Brief, Appellant asserts that the issues with respect to claim 31 differ from those addressed with respect to the rejection of claim 10. Reply Br. 19. Appellant also asserts that the Examiner has not shown that Bao's plating technique inherently "comprises placing a plating solution into contact with each conductive line exposed within the first dielectric layer" as recited in claim 31. *Id.* at 19–20.

Appellant's arguments are not persuasive of Examiner error. Appellant does not dispute the Examiner's finding (Final Act. 15) that Bao discloses plating capping layer 414 over the exposed surfaces of metal conductive lines 408 and 410. The record supports the Examiner's finding that Bao discloses plating techniques to plate capping layer 414. Bao ¶ 69. Appellant also does not dispute that Bao's Figure 4B discloses capping layer 414 on each conductive line exposed in Bao's Figure 4B.

Appellant's argument is essentially that because Bao discloses that there may be more than the two M_x metals depicted in the drawings, there is a possibility that not all of the additional M_x metals will be treated the same as the depicted M_x metals. Appeal Br. 39–40. Appellant's argument is not persuasive of error because it is inconsistent with Appellant's written description arguments. Appellant fails to adequately explain why one skilled in the art would not understand Bao's two depicted M_x metals to be representative of all exposed conductive lines. According to Appellant, a skilled artisan would understand the single conductive line depicted in Appellant's figures as representative of other conductive lines, which the skilled artisan would understand to be treated in the same manner, i.e., forming a capping layer using an electroless plating process, as in the single depicted conductive line. *Id.* at 20–23. According to Appellant, one skilled in the art would understand this to be the case because there are multiple conductive lines formed within the dielectric layer. *Id.* at 20. Similarly, Appellant represents that Bao discloses multiple conductive lines. *Id.* at 39–40 (citing Bao ¶ 66). Therefore, based on Appellant's representations regarding a person having ordinary skill in the art, we sustain the Examiner's rejection of claim 31 and its dependent claims under § 103.

CONCLUSION

For these reasons, we reverse the Examiner's rejections under 35 U.S.C. § 112(a) and affirm the Examiner's prior art rejections of claims 10, 12, 21–25, 30–34, and 37–44.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

DECISION SUMMARY

In summary:

Claims Rejected	**35 U.S.C. §**	**References/Basis**	**Affirmed**	**Reversed**
10, 12, 21–24, 37–44	112(a)	Written description		10, 12, 21–24, 37–44
31–34	112(a)	Written description		31–34
10, 12, 21–24, 37–44	103	Bao, Yu, Ballantine, Braeckelmann, Lopatin	10, 12, 21–24, 37–44	
25, 30	103	Bao, Braeckelmann, Ballantine	25, 30	
31–34	103	Bao, Ballantine, Bei, Yun	31–34	
Overall Outcome			10, 12, 21–25, 30–34, 37–44	

AFFIRMED