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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/870,594	09/30/2015	Todd RAFACZ	JRL-550-1910	7004

73459 7590 06/17/2020

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EXAMINER	
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ART UNIT	PAPER NUMBER
2145	

NOTIFICATION DATE	DELIVERY MODE
06/17/2020	ELECTRONIC

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte TODD RAFACZ and HUZEFA SANJELIWALA

Appeal 2019-001961
Application 14/870,594
Technology Center 2100

Before JOHN A. JEFFERY, JASON J. CHUNG, and CARL L. SILVERMAN, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Under 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–19. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM IN PART.

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as ARM Limited. Appeal Br. 3.

STATEMENT OF THE CASE

Appellant's invention categorizes access requests into regions for prefetching data. *See generally* Spec. 3–4. When an access request is received for a new, previously unrequested region, prefetch control circuity determines whether there is an adjacent region with a predetermined number of access request addresses. *See id.* 4–5. If a predetermined number of access request addresses exist for the adjacent region, then access request addresses to the new region are prefetched. *See id.* 5. Claim 1 is illustrative:

> 1. A prefetch apparatus comprising:
> access request reception circuitry to receive access requests, each access request having an access request address;
> request tracking storage to store a plurality of region entries, wherein each region entry corresponds to a region of memory space and corresponds to a plurality of access request addresses within that region of memory space,
> and wherein the request tracking storage is responsive to reception of each access request to update access information in its corresponding region entry;
> and prefetch control circuitry responsive to the access request reception circuitry receiving a new region access request which belongs to a new region for which there is no region entry,
> and when the request tracking storage has an adjacent region entry corresponding to an adjacent region of memory space to the new region for which the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed, to initiate a region prefetching process for all access request addresses in the new region.

THE REJECTIONS

The Examiner rejected claims 1–4, 8–11, 13, and 15–19 under 35 U.S.C. § 102(a)(1) as anticipated by de la Iglesia (US 2010/0115206 Al; published May 6, 2010). Final Act. 5–9.[2]

The Examiner rejected claims 5–7 and 12 under 35 U.S.C. § 103 as unpatentable over de la Iglesia and McCauley (US 2013/0346703 Al; published Dec. 26, 2013). Final Act. 9–11.

The Examiner rejected claim 14 under 35 U.S.C. § 103 as unpatentable over de la Iglesia and Dasika (US 2015/0121014 Al; published Apr. 30, 2015). Final Act. 11–12.

THE ANTICIPATION REJECTION

The Examiner finds that de la Iglesias discloses every recited element of independent claim 1 including the following:

> when the request tracking storage has an adjacent region entry corresponding to an adjacent region of memory space to the new region for which the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed, to initiate a region prefetching process for all access request addresses in the new region.

Final Act. 5–6. In the rejection, the Examiner maps the recited prefetch control circuitry to de la Iglesia's prefetch controller. *See* Final Act. 6. The Examiner also finds "at least a predetermined

[2] Throughout this opinion, we refer to (1) the Final Rejection mailed February 20, 2018 ("Final Act."); (2) the Appeal Brief filed July 16, 2018 ("Appeal Br."); (3) the Examiner's Answer mailed November 2, 2018 ("Ans."); and (4) the Reply Brief filed January 2, 2019 ("Reply Br.").

number of the access request addresses in the adjacent region of memory space have been accessed" is taught by de la Iglesia in that the total number of read and write blocks of an address region "are used to pre-fetch an address region different from the address region currently being accessed." *See id.* 12–13.

Appellant argues de la Iglesia's prefetch controller 18, prefetch table 34, and prefetch groups 40A and 40B do not teach the above-recited limitation. *See* Appeal Br. 8. According to Appellant, de la Iglesia's paragraph 39 fails to teach a predetermined number of access requests addresses in prefetch groups 40A or 40B. *See id.* Appellant further contends the number of accesses made to a memory's area in de la Iglesia fails to teach the recited "number of access request addresses." *See id.* 8–9. Appellant further argues de la Iglesia's confidence factor and area counter fail to teach the recited predetermined number of access request addresses. *See id.* 8. Appellant further contends the number of accesses to a memory taught in de la Iglesia does not teach the recited "number of access request addresses." *See id.* 8–9. Appellant further argues de la Iglesia's count register 256 indicates repeated access to a single memory address and thus cannot teach the recited predetermined number of the access request addresses. *See id.* 9. Appellant emphasizes the word "addresses" when quoting the disputed claim language, and contends that it is unreasonable to interpret the claim language to include a single access request address. *See id.* Appellant further argues "de la Iglesia is not concerned with the memory locations accesses within a region." *Id.* Appellant adds that determining how many blocks are

read and written in de la Iglesia's region 40 does not teach the determining "a predetermined number of the access request addresses in the region of memory space have been accessed." *See id.* Appellant further provides an example of de la Iglesia's register 228 recording 50 writes to the same access address, and contends that, in this example, the register would indicate a value of "50" despite accessing and writing to the same address. *See* Appeal Br. 9–10. Appellant adds that de la Iglesia's single register cannot store or track different access requests addresses for a larger memory space region (*see id.* 10), and that mapping multiple addresses to de la Iglesia's address region is improper. *See id.* Appellant further emphasizes the words "number of," "addresses," and "having been accessed," and argues de la Iglesia fails to teach the corresponding claim language. *See id.*

ISSUE

Under § 102, has the Examiner erred in rejecting claim 1 by finding that del la Iglesia discloses "when the request tracking storage has an adjacent region entry corresponding to an adjacent region of memory space to the new region for which the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed"?

ANALYSIS

We begin by construing the key disputed limitation of claim 1 that recites, in pertinent part "*when* the request tracking storage has an adjacent

region entry corresponding to an adjacent region of memory space to the new region for which the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed . . . ." (emphasis added). Our emphasis underscores that, when considered in context, the term "when" indicates that this is a conditional limitation. *See* MANUAL OF PATENT EXAMINING PROCEDURE (MPEP) § 2111.04(II) (9th ed. Rev. 08.2017, Jan. 2018) (citing *Ex parte Schulhauser*, Appeal 2013-007847 (PTAB Apr. 28, 2016) (precedential)). Although the limitations at issue in *Schulhauser* were rendered conditional by the recitation of "if" (*see Schulhauser* at 6–8), we nevertheless discern no meaningful distinction between the recitation of "if" and "when" in this context. One dictionary definition of "when" is "in the event that: IF." MERRIAM-WEBSTER'S COLLEGIATE DICTIONARY 1345–46 (1993).

For an apparatus claim, the broadest reasonable interpretation of a conditional limitation requires that the prior art disclose structure capable of performing the conditional limitation. *See Schulhauser* at 14, 15 ("[I]n order to show anticipation . . . of a claim reciting structure that performs a function tied to a condition precedent, the Examiner must cite prior art that discloses . . . such structure."); *see also* MPEP § 2111.04(II) (citing *Schulhauser*). On the other hand, a conditional limitation need not be satisfied to anticipate a method claim. *See Schulhauser* at 10 ("If the condition for performing a contingent step is not satisfied, the performance recited by the step need not be carried out in order for the claimed method to be performed."); *see also* MPEP § 2111.04 (II).

Here, because claim 1 is an apparatus claim, de la Iglesia must disclose a structure that can perform the elements in the recited "when" clause. But because independent claim 9 is a method claim, the recited "when" condition need not be satisfied for de la Iglesia to anticipate the claim. *See* MPEP § 2111.04 (II). Thus, even if we were to accept Appellant's contentions with respect to de la Iglesia's alleged failure to disclose the elements associated with the recited "when" condition—which we do not—these arguments are nevertheless incommensurate with the scope of claim 9 that does not require the "when" condition to be satisfied to anticipate the claim.[3]

Turning to the rejection, we first clarify the Examiner's mapping. First, the Examiner maps the recited "prefetch control circuitry" to de la Iglesias's prefetch controller 18. Final Act. 6. Second, the Examiner apparently maps the recited "receiving a new region access request which belongs to a new region for which there is no region entry" to de la Iglesia's teaching of an event that does not have an associated prefetch group. *See* Final Act. 6 (citing de la Iglesia paragraph 39 which teaches event 3's address range does not have a corresponding prefetch group).

The Examiner appears to map the "new region for which there is no region entry" to de la Iglesia's region 40B. *See* Final Act. 6 (citing paragraph 39 which teaches that region 40B is created in response to no prefetch group entry being associated with newly requested blocks 160–180).

[3] Although the scope and breadth of claim 9's conditional limitation is not dispositive here, we nonetheless raise this issue for the Examiner to consider after this opinion.

It appears the Examiner maps the recited "when the request tracking storage has an adjacent region entry corresponding to an adjacent region of memory space to the new region" to de la Iglesia's region 40A (i.e., the adjacent region) and 40B (i.e., the new region). *See* Final Act. 6 (citing paragraphs 78 and 79 that characterize 40A and 40B as "contiguously accessed blocks of storage"); *see also* de la Iglesia Fig. 5 element 20 (indicating adjacent regions 40A and 40B); *id.* ¶ 31 ("The aggregation combines transactions that occur in adjacent or overlapping block address ranges.").

The Examiner also apparently maps "for which the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed to initiate a region prefetching process for all access request addresses in the new region" to the number of access requests associated with region 40A. *See* Final Act. 6 (citing paragraph 78 teaching region 40B is prefetched when there is a storage access to any part of region 40A); Ans. 4 (citing Fig. 8 teaching in operation 330 "[i]f storage operation occurs to any part of Area 40A prefetch entire region 40B").

According to Appellant, de la Iglesia's prefetch controller 18 and prefetch table 34 with groups 40A and 40B in Figures 1 and 3 do not teach the disputed claim limitations. *See* Appeal Br. 8. Appellant adds that de la Iglesia's paragraph 39 does not teach the disputed claim limitations because "[t]here is no disclosure [that] a predetermined number of the access request addresses have been accessed in either the first or the second prefetch group 40A or 40B." *Id.*

These arguments are unavailing because not only are they incommensurate with the scope of the claim, these arguments do not persuasively rebut the Examiner's findings.

As noted above, operation 330 of de la Iglesias's Figure 8 is "[i]f storage operation occurs to any part of Area 40A, prefetch entire region 40B." Thus, if *any* request to access (i.e., storage operation) occurs to region 40A—a memory space region that is adjacent to region 40B as shown in de la Iglesias's Figure 5—then the *entire* region 40B, namely *all* access request addresss in that region is prefetched. Our emphasis on the word "any" underscores that de la Iglesias's operation 330 in Figure 8 prefetches the *entire* region 40B when indicating a *predetermined number* of access request addresses were accessed in adjacent region 40A, namely *at least one* access request address in region 40A.

To be sure, de la Iglesias's predetermined number of access request addresses is *necessarily* only one in operation 330, despite possibly being more than one as emphasized in the "at least one" language above. Nevertheless, nothing in the claim or the Specification precludes the recited predetermined number from being just one despite Appellant's arguments to the contrary. *See* Reply Br. 4–8. Not only is the term "predetermined" not defined in Appellant's Specification, unlike various other terms whose concrete definitions leave no doubt as to their meaning (*see, e.g.,* Spec. 19–20), we decline to import into the claim the particular embodiments that Appellant contends require the recited "predetermined number" to be two or more (*see* Reply Br. 5–7). *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned

against confining the claims to those embodiments. . . . [C]laims may embrace different subject matter than is illustrated in the specific embodiments in the specification.") (citations and internal quotation marks omitted). We also find unavailing Appellant's contention that de la Iglesia's confidence factor and area counter do not teach the recited predetermined number of access request addresses. *See* Appeal Br. 8. In short, this argument does not persuasively rebut the Examiner's reliance on the functionality of operation 330 in de la Iglesias's Figure 8 noted above. As shown in that figure, the confidence factor and area count are considered *before* operation 330 and are, therefore, merely precursors to indicating the predetermined number of access request addresses to adjacent region 40A in operation 330 as noted above.

Nor are we persuaded by Appellant's contention that "the number of accesses made to an area of memory is not the same as the number of access request addresses." Appeal Br. 8–9. Notably, each storage access operation (i.e., access request) in de la Iglesias has a corresponding address. *See* de la Iglesias ¶ 31 (teaching events are storage access operations); ¶ 38 (teaching events include address ranges). Thus, de la Iglesia teaches a number of access request addresses.

We likewise find unavailing Appellant's contention that de la Iglesia's count register only records requests to a single memory address (*see* Appeal Br. 9), and thus "no reasonable interpretation of this claim language understood in light of the specification by a person of ordinary skill in the art would encompass just a single access request address." *Id.* As noted above, nothing in the Specification or the claims requires excluding a single access

request from the recited "predetermined number."[4] *Accord* MPEP § 2111.01 (IV) ("The only exceptions to giving the words in a claim their ordinary and customary meaning in the art are (1) when the applicant acts as their own lexicographer; and (2) when the applicant disavows or disclaims the full scope of a claim term in the specification").

Turning to the Specification, the summary of claimed subject matter in the Appeal Brief includes citations from the Specification relevant to the recited "predetermined number." *See* Appeal Br. 3–4 (citing portions of pages 4–5 and 14–15[5] as support for the element that includes "predetermined number"). These portions of the Specification do not define the "predetermined number" unlike other terms whose concrete definitions leave no doubt as to their meaning. *See, e.g.,* Spec. 19–20. Nor does the Specification otherwise indicate that the predetermined number excludes one. *See* Spec. 4–5 (page 4 line 29 through page 5 line 4 characterizing the predetermined number as a threshold; page 14 line 16 through page 15 line 12 teaching an adjacent region accessed more than a defined threshold). Thus, although the Specification describes specific embodiments where the predetermined number is greater than one, the Specification nonetheless

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[4] As noted previously, the broadest reasonable interpretation of the recited predetermined number is *at least one* access request address, which includes not only one, but also more than one such address. Despite this breadth, to the extent that the Examiner interpretation of the recited predetermined number as *any possible number* of access request addresses (Ans. 4) somehow includes *zero* addresses, such an interpretation is unreasonable on this record. Nevertheless, we see no harmful error in the Examiner's articulated interpretation of the recited predetermined number to the extent that it is limited to *one or more* access request addresses.

[5] On page four of the Appeal Brief, it appears "page 5, line 12" is a typographical error and the correct citation should be "page 15, line 12."

does not explicitly exclude one from being the predetermined number. *See id.* Nor will we import these embodiments, let alone an unstated exclusion of one, into the claims. *See Phillips* 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments").

Nor does the word "addresses" in the context of claim 1 preclude the number one from being the recited predetermined number. For example, the request "[p]lease select a predetermined number of playing cards from the deck" does not exclude selecting only one card from the deck. The word "cards" merely indicates that a selection can include one or more cards.

Nor do we find availing Appellant's contention that "de la Iglesia is not concerned with the memory locations accessed within a region. . . ," and "determining the number of blocks read from or written to a particular address region 40 is not the same as determining that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed." Appeal Br. 9 (quotation marks and underlines omitted). Again, neither the claims nor the Specification excludes just one access address from the recited predetermined number of access request addresses. Region 40A in de la Iglesia is associated with a particular block range address (*see*, *e.g.*, de le Iglesia ¶ 38), and thus an access request to region 40A is an access request to at least one address.

Appellant's contention that de la Iglesia fails to teach determining "that at least of predetermined number of the access request addresses in the adjacent region of memory space have been accessed" (*see* Appeal Br. 9) is also unavailing. Even Appellant's own example—a hypothetical

embodiment with 50 writes to a single access address (*see id.* 9–10)—fully meets the recited predetermined number of access request addresses, namely one. Notably, a region access in de la Iglesia's region 40A is not confined to any particular number of read or write operations. *See* de la Iglesia ¶ 78 (teaching *a* storage access in any part of region 40A).

Appellant's additional contention with respect to the feasibility of de la Iglesia's register to "store all the data necessary to track how many different access request addresses have been accessed for a larger region of memory" (*see* Appeal Br. 10) is also unavailing because this argument is not commensurate with scope of the claim language. The claim does not require *many* different access request addresses: it requires indicating that *a predetermined number* of access request addresses have been accessed. As noted above, de la Iglesia teaches the recited predetermined number because, among other things, it teaches at least one access request address in the adjacent region of memory space (i.e., region 40A). *See* de la Iglesia ¶¶ 38, 78–79; Fig. 8 (operation 330).

Nor do we find availing Appellant's contention that de la Iglesia fails to teach "using a predetermined number of access request addresses in an adjacent region having been accessed to initiate prefetching a region prefetching process for all access request addresses in the new region." *See* Appeal Br. 10 (underlining in original). As emphasized above, the recited "have been accessed" language is in the past tense: thus, the claim requires indicating a predetermined number of access request addresses that *have been* accessed (i.e., that were accessed previously).

As noted previously, de la Iglesias's operation 330 in Figure 8 prefetches the entire region 40B responsive to indicating a predetermined

number of access request addresses, namely at least one such address, *was* accessed in adjacent region 40A. Our emphasis on the term "was" underscores that indicating the predetermined number of access request addresses—even just one—in region 40A occurs *before* prefetching the entire region 40B in operation 330 of de la Iglesias's Figure 8. *See* de la Iglesias ¶ 78. That is, even if just one access request address in region 40A was accessed in de la Iglesias's operation 330, the prefetch of all such addresses in region 40B would not occur *but for* indicating that the address in region 40A was accessed.

Appellant's arguments in the Reply Brief are also unavailing. *See* Reply Br. 2–8. First, Appellant's contention that the Examiner's delayed explanation in the Answer ostensibly violates a section of the MPEP pertaining to compact prosecution (*see* Reply Br. 3 (citing MPEP § 2103 (I)) is a petitionable matter that is not before us. *See* MPEP § 706.01 ("[T]he Board will not hear or decide issues pertaining to objections and formal matters which are not properly before the Board."); *see also* MPEP § 1201 ("The Board will not ordinarily hear a question that should be decided by the Director on petition . . . ."); MPEP § 1207.03(b) ("37 CFR 41.40 sets forth the exclusive procedure for an appellant to request review of the primary examiner's failure to designate a rejection as a new ground of rejection via a petition to the Director under 37 CFR 1.181").

Appellant also argues the existence of a region entry already indicates that one access occurred to a region and, therefore, it ostensibly does not make sense to also provide information that an access request has been made to the region. *See* Reply Br. 4. This argument is unavailing because it ignores de la Iglesia's teaching that access request addresses are recorded for

region 40A. *See* de la Iglesia ¶ 55 (indicating that storage operations (i.e., requests to read and write) are recorded for address region 40A). Even assuming, without deciding, that the access request information in de la Iglesia is redundant, that would not still not preclude de la Iglesia from anticipating the claim.

Appellant also argues that the Specification provides guidance that the scope of the recited predetermined number cannot include one. *See* Reply Br. 5–7. The disclosure cited by Appellant includes embodiments that involve a "plurality of access requests" (*see id.* 5); "counting the number of set access indications" (*see id.*); "a sufficient number of [] access request[s]" (*see id.*); and 13 address accesses. *See id.* 6–7.

Although this disclosure informs our understanding of the recited predetermined number, we decline to import these disclosed embodiments into the claims. *See Phillips* 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments); *see also* MPEP § 2111.01 (II). ("Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim."). Additionally, unlike various terms that are defined explicitly (*see, e.g.,* Spec. 19–20), the Specification does not define the recited predetermined number or otherwise limit the number to more than one. Thus, again, we are not persuaded that the claims or the Specification exclude the number one from the recited predetermined number.

Appellant's argument that de la Iglesia does not teach a predetermined number of one (*see* Reply Br. 7) is also unavailing. For example, Figure 8

operation 330 of de la Iglesia teaches prefetching 40B if *any* part of Area 40A is accessed. The word "any" teaches a determination of at least one access request.

Appellant's argument that de la Iglesia fails to teach a "number of access requests" because the read and write registers are not added together (*see* Reply Br. 8) is also unavailing. As previously indicated, de la Iglesia teaches at least one access request to region 40A (*see, e.g.*, Fig. 8 operation 330operation 330) and therefore teaches the predetermined number of access requests includes at least one.

Appellant's argument that de la Iglesia does not compare a number of access requests to the specific value of one is also unavailing because the arguments are not commensurate with the scope of the claim language. That is, the claim does not recite "comparing." But even if it did, operation 330 of de la Iglesia's Figure 8 teaches prefetching 40B if *any* part of Area 40A is accessed. Requiring a determination of whether *any* part of Area 40A is accessed requires logically comparing an access request to a threshold of at least one.

Appellant's argument that de la Iglesias fails to teach "the access information indicates that at least a predetermined number of the access request addresses in the adjacent region of memory space have been accessed" because paragraphs 71, 73, and 74 merely teach that the number of read and write blocks are "used" (*see* Reply Br. 8) is also unavailing. Not only does this contention fail to persuasively rebut the functionality of operation 330 in de la Iglesias's Figure 8 that indicates that at least one access request addresses was accessed in region 40A as explained above, the storage operations in de la Iglesia are also characterized as a "sequence of

accesses." *See* ¶ 37. Thus, storage operations represent addresses that have been accessed

Therefore, for the reasons indicated above, we are not persuaded that the Examiner erred in rejecting claim 1, and claims 2–4, 8–11, 13, and 15–19 not argued separately with particularity.

THE OBVIOUSNESS REJECTION OVER DE LA IGLESIA AND MCCAULEY

Claim 7

In rejecting dependent claim 7, the Examiner cites McCauley paragraphs 38 through 39, paragraph 42, and Figure 6 element 605 as teaching, among other things, (1) a region tag; (2) an offset in an offset range; (3) an upper half of an offset range; and (4) a lower half of an offset range. *See* Final Act. 10. The Examiner further finds addresses above or below a line offset are examined based on McCauley's direction bit and line offset. *See* Ans. 5–6 (citing McCauley ¶ 42).

Appellant argues McCauley teaches a line offset, but fails to teach the remaining elements of claim 7. *See* Appeal Br. 11.

ISSUE

Under § 103, has the Examiner erred in rejecting claim 7 by finding that de la Iglesias and McCauley collectively teach or suggest "a region tag"; "an offset in an offset range"; and "the offset being in a lower half of the offset range to examine the access information in the adjacent region of memory space below the access request address and is responsive to the offset being in a upper half of the offset range"?

ANALYSIS

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. *See also In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements. "), *quoted with approval in KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Here, we are persuaded that the Examiner's obviousness rejection of claim 7 is deficient because the Examiner's findings in the Final Rejection and the Answer fail to address adequately the elements of claim 7 recited above. *See* Final Act. 10; Ans. 5–6. For example, there is no mapping of the recited region tag or the upper and lower half of the offset range. *See* Final Act. 10; Ans. 5–6. Consequently, we are left to speculate regarding what exactly constitutes these elements in the prior art.

McCauley's paragraphs 38 and 39 teach, among other things, a 40-bit physical address, a page address, a line offset for address 505, and a direction bit, but we fail to see—nor has the Examiner shown—how these elements teach or suggest a region tag and an upper or lower half of an offset range as claimed. Nor does the Final Rejection and Examiner's Answer articulate any specific mapping of these recited features, let alone explain why these features would have been obvious. *See* Final Act. 10; Ans. 5–6. McCauley Figure 6 shows that stream entries 605 include, among other things, a page address, line offset, prefetch flags, direction bit, initial line offset, and access history, but, again, the Examiner fails to show these elements or their accompanying disclosure teaches or suggests the region tag or upper and lower half offset ranges, let alone explain why these features

would have been obvious. *See* Final Act. 10; Ans. 5–6. Nor will we speculate in that regard here in the first instance on appeal.

In response to Appellant's argument that McCauley fails to teach the above recited elements of claim 7 (*see* Appeal Br. 11–10), the Examiner finds that McCauley's line offset and direction bit cause addresses to be examined above and below the line offset. *See* Ans. 5–6. Again, the Examiner does not articulate any specific mapping of the recited region tag or the recited upper and lower half offset ranges, let alone explain why these features would have been obvious. *See* Final Act. 10; Ans. 5–6. Appellant additionally points out, and we agree, that there is no teaching in McCauley where the offset is in the recited offset range, let alone prefetch control circuitry that is responsive to the particular location of that offset as claimed. *See* Reply Br. 9–10.

Because the Examiner has not shown that McCauley teaches or suggests the recited elements of claim 7, or that de la Iglesias cures that deficiency, we are persuaded that the Examiner erred in rejecting dependent claim 7.

Claims 5, 6, and 12

We do, however, sustain the Examiner's obviousness rejection of claims 5, 6, and 12. Final Act. 9–11. Because the rejection of these claims is not argued separately with particularity, we are not persuaded of error in the rejection of these claims for the reasons previously discussed.

THE OBVIOUSNESS REJECTION OVER DE LA IGLESIA AND DASIKA

We also sustain the Examiner's obviousness rejection of claim 14 over de la Iglesias and Dasika. Final Act. 11–12. Because this rejection is not argued separately with particularity, we are not persuaded of error in this rejection for the reasons previously discussed.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s) /Basis	Affirmed	Reversed
1–4, 8–11, 13, 15–19	102(a)(1)	de la Iglesia	1–4, 8–11, 13, 15–19	
5–7, 12	103	de la Iglesia, McCauley	5, 6, 12	7
14	103	de la Iglesia, Dasika	14	
Overall Outcome			1–6, 8–19	7

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED IN PART