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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MURUGASAMY K. NACHIMUTHU,
MOHAN J. KUMAR, and GEORGE VERGIS

Appeal 2019-001926
Application 14/748,798
Technology Center 2100

Before MAHSHID D. SAADAT, ALLEN R. MacDONALD, and NABEEL U. KHAN, *Administrative Patent Judges.*

MacDONALD, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–25. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Intel Corporation. Appeal Br. 3.

CLAIMED SUBJECT MATTER

Claim 1 is illustrative of the claimed subject matter (emphasis, formatting, and bracketed material added):

> 1. A method for saving data in dynamic random access memory (DRAM) in a computer platform to a persistent storage device, wherein the computer platform includes a primary power source used to provide power to components in the computer platform during normal operation, the computer platform including the persistent storage device and running an operating system during normal operation, the method comprising:
>
> [A]. detecting a power unavailable condition under which power is no longer being supplied by the primary power source to the computer platform; and, in response to detection of the power unavailable condition,
>
> [B]. automatically copying data in the DRAM to the persistent storage device without operating system intervention,
>
> [C]. ***wherein the DRAM comprises one or more volatile DRAM dual in-line memory modules (DIMMs) and the persistent storage device is separate from the one or more volatile DRAM DIMMs***.

REFERENCES

The Examiner relies on the following prior art:

Name	Reference	Date
Kelly	US 2016/0118121 A1	Apr. 28, 2016
Judd	US 2014/0215277 A1	July 31, 2014
McKelvie	US 9,535,828 B1	Jan. 3, 2017
McKnight	US 2012/0131253 A1	May 24, 2012
Davis	US 2013/0089104 A1	Apr. 11, 2013
Fullerton	US 2009/0287902 A1	Nov. 19, 2009

REJECTIONS[2]

A.

The Examiner rejects claims 1–3, 7, and 8 under 35 U.S.C. § 103 as being unpatentable over Kelly, in view of Judd or McKelvie.[3] Ans. 4–6.

Appellant does not separately argue claims 2, 3, 7, and 8, and instead relies upon its argument regarding claim 1. *See* Appeal Br. 24. Except for our ultimate decision, we do not discuss the § 103 rejection of claims 2, 3, 7, and 8 further herein.

B.

The Examiner rejects claims 4–6 and 9–25 under 35 U.S.C. § 103 as being unpatentable over Kelly, in view of Judd or McKelvie, and further in view of McKnight, Davis, or Fullerton. Ans. 6–9.

Appellant does not separately argue claims 6, 10–17, 20–22, and 25, and instead either relies upon its argument regarding one of claims 1, 5, 9, 12, and 19, or does not address the respective claim. *See* Appeal Br. 25–43. Except for our ultimate decision, we do not discuss the § 103 rejection of claims 6, 10–17, 20–22, and 25 further herein.

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[2] In the Final Office Action, the Examiner also rejected claims 1–9 under 35 U.S.C. § 112(a) as failing to comply with the written description requirement. *See* Final Act. 6. However, the Examiner failed to carry over the rejection in the Examiner's Answer. *See generally* Ans. Therefore, we treat the rejection of claims 1–9 under 35 U.S.C. § 112(a) as withdrawn.

[3] Although the Final Action (page 7) and Answer (page 4) list claims 1–9 as covered by this rejection, only claims 1–3, 7, and 8 are actually so rejected. Final Act. 7–10; Ans. 4–6.

OPINION

We have reviewed the Examiner's rejections in light of Appellant's Appeal Brief and Reply Brief arguments.

A. Claim 1

Appellant raises the following argument in contending the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103.

> Kelly discloses use of NVDIMMs (Non-Volatile Dual Inline Memory Modules). ***A DRAM DIMM is not an NVDIMM and vice versa.*** This is well-known in the computer system art and data center art (NVDIMMs are commonly used in data centers). Applicant discusses operation of NVDIMMs in the present application, and it is well-known that NVDIMMs are used to write memory from DRAM to NV memory (typically flash) without operating system intervention, as the DRAM and the NV memory are on the same DIMM device.
>
> . . . .
>
> [U]nder Kelly, conventional NVDIMM operations are disclosed. These are similarly discussed in the present application (see, e.g., paragraph [0005]). ***The difference in Kelly is that Kelly's NVDIMM doesn't include a battery or super-capacitor; however, both the volatile DRAM and non-volatile memory are on the same NVDIMM devices.***

Appeal Br. 14–17 (emphasis added); *see also* Reply Br. 4–6.

We are unpersuaded by Appellant's argument. We agree with the Examiner that Kelly teaches all the elements of claim 1 except for the claimed "one or more volatile DRAM dual in-line memory modules (DIMMs)," and the claimed "persistent storage [being] separate from the one or more volatile DRAM DIMMs." *See* Ans. 4 (citing Kelly ¶¶ 169, 172, 176, 185, 202). We further agree with the Examiner that Judd teaches the aforementioned elements of claim 1. *See* Ans. 4 (citing Judd ¶¶ 64, 70). Appellant's argument that Kelly's non-volatile DIMM (NVDIMM) does not

teach or suggest the claimed "one or more volatile DRAM dual in-line memory modules (DIMMs)," does not address the Examiner's combination of Kelly and Judd, as the Examiner relied upon Judd rather than Kelly for teaching or suggesting the aforementioned element of claim 1. One cannot show non-obviousness by attacking references individually when the rejection is based on a combination of references. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *see also In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

Appellant also raises the following argument in contending the Examiner erred in rejecting claim 1.

> ***The Examiner fails to identify how Kelly would be modified by Judd.*** In particular, there is no discussion in the rejection concerning how this might be done.
>
> . . . .
>
> The Examiner's alleged motivation to combine Kelly with Judd, "in order to save space on the DIMM and reduce the need to incur the cost of additional system memory," ***is also unrelated to the claimed invention of claim 1, as well as not providing any benefit***. Kelly already discloses an NVDIMM, which has the same JEDEC (Joint Electron Device Engineering Council) standard physical interface and form factor as a DIMM, and has the same system memory (DRAM) as a DIMM of similar capacity.
>
> . . . .
>
> Moreover, [a] single NAND Flash chip has twice the storage . . . as DRAM[.] ***There would be nothing accomplished by saving space on a DIMM by removing the NAND Flash chip, and there would be no reduced cost of system memory through use of Judd since that same amount of system memory (depicted as the DRAM chips) would already be on the NVDIMM of Kelly. Substituting Judd's DRAM DIMM for Kelly's NVDIMM under Kelly's architecture also would lead to***

> ***an inoperable result, and a PHOSITA would have no reason to attempt to so.***

Appeal Br. 17–19 (emphasis added); *see also* Reply Br. 6–18.

We are unpersuaded by this argument as well. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d at 425 (citations omitted); *see also In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) ("Combining the teachings of references does not involve an ability to combine their specific structures."). We agree with the Examiner that the motivation to make the modification (i.e., the replacement of the NVDIMM of the memory data save system disclosed in Kelly with the DIMM and external non-volatile storage disclosed in Judd) is found in Judd itself, as Judd discloses having an external non-volatile storage advantageously saves space on the DIMM and reduces the need to incur the cost of additional system memory. *See* Ans. 10 (citing Judd ¶ 64). Contrary to Appellant's argument, this motivation is related to the claimed invention, as Appellant's Specification discloses that one advantage of the claimed invention is increased available memory on the DIMMs. *See, e.g.*, Spec. ¶ 80 ("standard DRAM DIMMs are used rather than NVDIMMs, hence the OS visible persistent memory size is the same as the DRAM size, thus overall memory available to workload is not reduced as compared to DRAM"). Further, Appellant's argument that it presented fact-based evidence that substituting the DIMM of Judd for the NVDIMM of Kelly would not save space on the DIMM and reduce the need to incur cost of additional system memory is not

persuasive, as it contradicts the aforementioned disclosures of Appellant's Specification and Judd.

Appellant further argues that McKelvie fails to teach or suggest automatically copying data in a DRAM to a persistent storage device upon detection that power is no longer being supplied by a primary power source because McKelvie solely discloses writing RAM to a persistent storage device when power is available. *See* Appeal Br. 19–23; *see also* Reply Br. 18–19. Appellant additionally argues the Examiner fails to provide details as to how Kelly would be motivated by McKelvie or how the teachings of Kelly, Judd, and McKelvie could be combined to obtain the invention of claim 1. *See* Appeal Br. 23; *see also* Reply Br. 19–21. These arguments are also not persuasive because the Examiner relies upon McKelvie as an alternative to Judd, and we do not reach the Examiner's findings regarding McKelvie, as we sustain the Examiner's findings that the combination of Kelly and Judd teach or suggest all the elements of claim 1.

B. Claim 4

Appellant raises the following argument in contending the Examiner erred in rejecting claim 4.

> The foregoing ***says nothing about a power protected direct memory access (DMA) engine or programming the power protected DMA engine to copy data in the DRAM to the persistent storage device***. It is merely some boilerplate language that is very general in nature, and doesn't provide any details on how direct memory access would be implemented, other than it may be used to communicate technical data and/or technical instructions. ***Kelly provides no disclosure concerning saving DRAM data using DMA***. Moreover, ***Kelly discloses use of a NVDIMM for saving DRAM data, wherein the DRAM is on the same NVDIMM device.***
>
> . . . .

> McKnight clearly discloses use of NVRAM (non-volatile RAM) and NVDIMMs, ***both of which are clearly not volatile DRAM DIMMs***. In addition, ***NVRAM is not DRAM***, as would be recognized by a PHOSITA.
>
> . . . .
>
> The DMA & VMM support 224 and paragraph [0029] [of Davis] ***do not teach or suggest a power protected direct memory access (DMA) engine or programming the power protected DMA engine to copy data in the DRAM to the persistent storage device***.
>
> . . . .
>
> Not only do none of the reference teach use of "a power protected direct memory access (DMA) engine," ***none of the references teach programming a DMA engine of any sort to copy data in the DRAM to the persistent storage device***.

Appeal Br. 26–28 (emphasis added); *see also* Reply Br. 21–22.

We are not persuaded by Appellant's argument. As the Examiner correctly found, Kelly discloses a computer system that communicates technical data and/or instructions through direct memory access (DMA). *See* Ans. 6, 17 (citing Kelly ¶ 134). As the Examiner also correctly found, McKnight discloses: a peripheral component interconnect express (PCIe)-to-double data rate (DDR) interface logic that includes a system-to-card (S2C) DMA engine which manages data transfer from system memory to DDR memory of the NVDIMMs (i.e., DMA write operations) and a card-to-system (C2S) DMA engine which manages data transfers from DDR memory to a host system memory (i.e., DMA read operations); and a power generation and detection logic that provides required voltage to power the PCIe-to-DDR interface logic. *See* Ans. 7, 17 (citing McKnight ¶ 6); *see also* McKnight ¶¶ 20, 26, 27, 29. Even further, as also correctly found by the Examiner, both Davis and Fullerton discloses low power DDR RAM, which

facilitates direct access memory for the overall computing system. *See* Ans. 7, 17 (citing Davis ¶ 30; Fullerton ¶ 21). In light of Kelly's disclosure of communicating data through DMA, McKnight's disclosure of copying data in system memory to DDR memory, and Davis and Fullerton's disclosure of programming power to a DDR RAM of an overall computing system, we agree with the Examiner that the combination of Kelly, McKnight, Davis, and Fullerton teaches or suggests the claimed "programming the power protected DMA engine to copy data in the DRAM to the persistent storage device." *See* Ans. 17.

Appellant also raises the following argument in contending the Examiner erred in rejecting claim 4.

> [The Examiner's rationale] ***doesn't even hint at a suggestion of how the Kelly, Judd, McKelvie McKnight, Davis, and Fullerton references could be combined*** to obtain the invention of claim 4, nor ***why a PHOSITA would be motivated to do so*** (based on what is actually disclosed in Kelly, Judd, McKelvie McKnight, Davis, and Fullerton), nor ***why a PHOSITA would have any expectation of success***.
>
> . . . .
>
> In adding Fullerton, the Examiner has provided no evidence to ***why a PHOSITA would look to Fullerton at all***.

Appeal Br. 29 (emphasis added); *see also* Reply Br. 23.

This argument is unpersuasive as well. As previously described, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, or whether the specific structures of the references can be physically combined. Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *See in re Keller*, 642 F.2d at 425. Regarding motivation, the Examiner found that one of ordinary skill in

the art would have been motivated to incorporate the aforementioned features of McKnight, Davis, and Fullerton in order to provide guaranty of data durability. *See* Ans. 7. Thus, contrary to Appellant's argument, the Examiner has provided a motivation to modify the computer system disclosed in Kelly to incorporate the aforementioned features of McKnight, Davis, and Fullerton.

C. Claim 5

Appellant raises the following argument in contending the Examiner erred in rejecting claim 5.

> With respect to Kelly, the reference to direct memory access in paragraph [0134] ***has nothing to do with saving data in DRAM to a persistent storage device, which is performed using an NVDIMM, wherein the NVDIMM includes both the DRAM and the persistent storage device (NAND memory).*** With further respect to PCIES 136, these correspond to PCIe devices 136, ***which are not used for any purpose by Kelly in connection with saving data in DRAM to a persistent storage device***.
>
> . . . .
>
> With respect to McKnight, the Examiner alleges a DDR2 link is an IO link (that is apparently coupled to an IO interface). ***A person having ordinary skill in the art (PHOSITA) would not consider a DDR2 link to be an IO link within the context of the meaning of an IO link in claim 5, which is separate and apart from the first memory controller, which a PHOSITA would recognize is coupled to a memory device via a memory link***. DDR2 stand for double data rate 2nd generation, which corresponds to a standardized memory link. Thus, a PHOSITA would recognize the DDR2 links as memory device links (i.e., links between a memory controller and a memory device). For example, Figure 2 of McKnight shows a DDR2 controller, which is a DDR2 memory controller used to access DDR2 memory.
>
> . . . .

> ***The Examiner has not identified how the teachings of Kelly and McKnight would be combined, nor why a PHOSITA would have any motivation to combine Kelly and McKnight or have any reasonable expectation of success in doing so.***
>
> Under claim 5, the persistent storage device is coupled to an IO link that is separate from a first memory controller-to-DRAM device link (original claim language, now a first memory controller-to-DRAM DIMM link), Under both of Kelly and McKnight, the persistent storage device is an NVDIMM, which is clearly coupled to some sort of memory link in each of Kelly (unspecified) and McKnight (DDR2 link).

Appeal Br. 36–38 (emphasis added); *see also* Reply Br. 25–29.

We are unpersuaded by Appellant's argument. Contrary to Appellant's argument that the cited paragraph of Kelly has nothing to do with saving data in DRAM to a persistent storage device, Kelly discloses backing up data in a DRAM to a non-volatile memory and further discloses that technical data and/or technical instructions may be communicated through direct memory access. *See* Ans. 7, 21 (citing Kelly ¶¶ 134, 176, 202). To the extent that Appellant is arguing that Kelly's NVDIMM does not teach or suggest the claimed "IO link coupling the persistent storage device to the IO interface" because Kelly's NVDIMM includes both the DRAM and the persistent storage device, this argument does not address the Examiner's combination of Kelly and Judd, as the Examiner relied upon Judd rather than Kelly for teaching the persistent storage being separate from the NVDIMM. *See* Ans. 4.

Further, Appellant's argument fails to persuasively establish that one of ordinary skill in the art would not consider McKnight's double data rate (DDR2) link to be an IO link as Appellant fails to identify the characteristics of the claimed "IO link" that allegedly distinguish it from McKnight's

DDR2 link. Even assuming *arguendo* that McKnight's DDR2 link does not teach or suggest the claimed "IO link," Judd also teaches or suggests the aforementioned limitation as Judd discloses "[a] Serial Attached Small Computer System Interface (SAS) [that connects] an external storage drive to the DIMM." Judd ¶ 64. Appellant's argument does not address the SAS interface disclosed in Judd, and thus, is not persuasive. Even further, Appellant's argument regarding the Examiner's combination of Kelly and McKnight is also not persuasive for the reasons previously described with respect to the rejection of claim 4.

D. Claim 9

Appellant raises the following argument in contending the Examiner erred in rejecting claim 9.

> As is well-known in the processor art, SMM and SMI are associated with Intel® processors (and AMD processors) employing the x86 architecture (see, e.g., https://en.wikipedia.org/wiki/System_Management_Mode). ***Paragraphs [0202] and [0341] of Kelly [have] nothing to do with SMI or SMM. The FPGA of McKnight clearly is not a processor that supports SMI or SMM.*** Broadest reasonable interpretation of claim must be in consideration of both the specification and drawings of the patent application and what was known in the art at the time of the invention. ***BRI does not include the broadest possible interpretation, nor allow an examiner to ignore claim limitations that are well-known in the art.***

Appeal Br. 30 (emphasis added); *see also* Reply Br. 23–24.

We are not persuaded by Appellant's argument. As the Examiner correctly found, McKnight discloses a field programmable gate array (FPGA) of a non-volatile RAM (NVRAM) device that manages a data transfer between a host system and the NVRAM device. *See* Ans. 8 (citing

McKnight ¶ 25). As disclosed in McKnight, in an event a supply power from a PCIe bus drops below a threshold reference level, an interrupt is provided to the FPGA, and, in response, the FPGA initiates the data back-up process. *See* McKnight ¶ 23. Although Appellant argues the claimed "System Management Interrupt (SMI) and one or more System Management Mode (SMM) handlers," is patentably distinct from McKnight's FPGA interrupt and FPGA interrupt handlers, Appellant fails to specifically identify the characteristics of the claimed "SMI" and "SMM handlers" that allegedly distinguish it from McKnight's FPGA interrupt and FPGA interrupt handlers.

E. Claim 18

In contending the Examiner erred in rejecting claim 18, Appellant argues "[t]here is nothing in [Kelly] that says the links to any NVDIMMs are power protected links," and "[t]he electrical connections to provide power to NVDIMMs are not considered IO (input-output) links in the art - there is no IO data sent over these [electronic] connections, only voltage." Appeal Br. 32; *see also* Reply Br. 24–25. This argument is unpersuasive. As correctly found by the Examiner, Davis discloses a computing system that includes one or more processing cores, and I/O interfaces. *See* Ans. 20 (citing Davis ¶ 160); *see also* Davis ¶ 29. As also correctly found by the Examiner, Kelly discloses reducing power to select components during a backup/save operation. *See* Ans. 20 (citing Kelly ¶ 202 ("during this backup/save operation, except for the NVDIMMs, all other server components . . . can be powered down")). Furthermore, Judd discloses a backup power source providing power to a high speed interface to allow for data transfer upon detection of primary power unavailability. *See* Judd ¶¶ 55, 64 ("[h]igh speed

interfaces such as SATA and SAS are preferred in order to . . . [minimize] the energy required from the backup power source," "when the primary power source of the computer system fails (S51), the Backup power source supplies power for a short period," "[a] Serial Attached Small Computer System Interface (SAS) is suitable for connecting an external storage drive to the DIMM"). Appellant's argument does not address the aforementioned disclosures of Judd, and thus, is not persuasive.

F. Claim 19

Appellant raises the following argument in contending the Examiner erred in rejecting claim 19.

> Each of claims 19 and 25 refer to updating of updating meta-data stored in the persistent storage device to indicate the data has been successfully saved to the persistent storage device. ***This limitation is not included in any of claims 1-9, nor is such a limitation taught by any of Kelly, McKnight, Davis, or Fullerton.*** . . . The Examiner ***failed to comment on the rejection of claims 19 and 25*** in his Response to Arguments, and has ***failed to address the limitation in claims 19 and 25*** in either the Final Office Action or the prior Non-final Office Action.

Appeal Br. 39–40 (emphasis added); *see also* Reply Br. 27.

We have considered this argument, but we are not persuaded that the Examiner erred in rejecting claim 19. In rejecting claim 19, the Examiner indicated that "the rationale in the rejection of claims 1–9 is incorporated." Ans. 9. As part of rejecting claim 1, the Examiner relied upon Judd, citing paragraphs 64 and 70. *See* Ans. 4–5 (citing Judd ¶¶ 64, 70). These paragraphs of Judd disclose backing up data stored within a DRAM to an external persistent storage device in the vent of a failure of a primary power source. *See* Judd ¶ 64. Judd further discloses that, as part of this backup, metadata is also stored within the external persistent storage device. *See*

Judd ¶ 60. Further, as part of rejecting claim 1, the Examiner alternately relied upon McKelvie, citing column 8, lines 29–45. *See* Ans. 5 (citing McKelvie 8:29–45). This portion of McKelvie also discloses backing up data stored in volatile memory to a non-volatile memory in the event of a failure. *See* McKelvie 8:29–45. McKelvie further discloses that metadata or log information is also stored with the data within the non-volatile memory. *See* McKelvie 5:64–67. In light of the fact that both Judd and McKelvie disclose storing metadata along with the underlying data in the persistent storage device, Appellant has not shown the Examiner erred in rejecting claim 19 as obvious over the combination of the cited prior art references.

G. Claim 23

Regarding claim 23, Appellant argues "[a]n APIC (Advance Programmable Interrupt Controller) is a particular type of interrupt controller used in INTEL® processors and has a well-known meaning within the processor arts," and "[w]hat is described in Davis ¶0149, 0160 is not an APIC, as the term is known in the art." Appeal Br. 33; *see also* Reply Br. 25. This argument is not persuasive. As the Examiner correctly found, Davis discloses an interrupt controller that is extended beyond its standard functional parts. *See* Ans. 20 (citing Davis ¶ 160). Although Appellant argues the claimed "APIC (Advance Programmable Interrupt Controller)" is patentably distinct from Davis's interrupt controller, Appellant fails to specifically identify the characteristics of the claimed "APIC" that allegedly distinguish it from Davis's interrupt controller.

H. Claim 24

With respect to claim 24, Appellant argues "claim 24 requires processors to be installed in the sockets, and the socket-to-socket interface to

be on the processor," and "[t]he sockets in McKnight are sockets in which the NVDIMMs are installed, and have nothing to do with the sockets in claim 24, nor the socket-to-socket interface in claim 24." Appeal Br. 34; *see also* Appeal Br. 43; Reply Br. 25. We are unpersuaded by Appellant's argument. As the Examiner correctly found, McKnight discloses a controller configured to manage data transfers between a host and a specified socket of a set of NVDIMM sockets in which an NVDIMM card is accommodated as DMA reads and writes. *See* Ans. 20–21 (citing McKnight ¶ 6). As further disclosed in McKnight, a field programmable gate array (FPGA) and associated logic is configured to facilitate the aforementioned data storage operations, and more specifically, is configured to facilitate high speed PCIe-based DMA to a DDR2 NVDIMM. *See* McKnight ¶ 20, Fig. 2. Even more specifically, McKnight discloses that the PCIe-to-DDR interface logic is instantiated in the FPGA between the PCIe end point 34 and DDR2 controller, and is responsible for managing the register read and write operations. *See* McKnight ¶ 26, Fig. 7. Although Appellant argues the claimed "sockets" and "socket-to-socket interconnect interface" are patentably distinct from McKnight's NVDIMM sockets and PCIe-to-DDR interface, Appellant fails to specifically describe how the claimed "sockets" and "socket-to-socket interconnect interface" are distinct from McKnight's NVDIMM sockets and PCIe-to-DDR interface.

CONCLUSION

The Examiner has not erred in rejecting claims 1–25 as being unpatentable under 35 U.S.C. § 103.

The Examiner's rejections of claims 1–25 as being unpatentable under 35 U.S.C. § 103 are **affirmed**.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	References/Basis	Affirmed	Reversed
1–3, 7, 8	103	Kelly, Judd, McKelvie	1–3, 7, 8	
4–6, 9–25	103	Kelly, Judd, McKelvie, McKnight, Davis, Fullerton	4–6, 9–25	
Overall Outcome			1–25	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED