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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES BAUMAN

Appeal 2019-001893
Application 15/378,473
Technology Center 2100

Before KALYAN K. DESHPANDE, CHARLES J. BOUDREAU, and SHARON FENICK, *Administrative Patent Judges*.

BOUDREAU, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 21–40, which are all of the pending claims. We have jurisdiction under 35 U.S.C. § 6(b)(1).

We REVERSE.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies Advanced Micro Devices, Inc. as the real party in interest. Appeal Br. 1.

CLAIMED SUBJECT MATTER

Appellant's invention relates to "an interface for coupling flash memory and dynamic random access memory in processing systems." Spec. ¶ 2.

Claims 21, 27, and 35 are independent. Claim 21, reproduced below, is illustrative of the subject matter on appeal (emphasis added):

> 21. A memory system, comprising:
>
> a dynamic random access memory (DRAM);
>
> a flash memory; and
>
> ***a dedicated interface between the DRAM and the flash memory***, wherein a first portion of the dedicated interface is implemented in the DRAM and a second portion of the dedicated interface is implemented in the flash memory, and further ***wherein the dedicated interface is only available for communication between the flash memory and the DRAM***.

Appeal Br. 11 (Claims App.).

REJECTION

Claims 21–40 stand rejected under 35 U.S.C. § 102(a)(1) as being anticipated by Lee.[2] Final Act. 5–7.

OPINION

The Examiner finds, *inter alia*, that Lee teaches "a dedicated interface between the DRAM and the flash memory" that "is only available for communication between the flash memory and the DRAM," as recited in independent claim 21 and similarly recited in independent claims 27 and 35. Final Act. 5–6 (citing Lee ¶ 86, Figs. 3–5). Specifically, the Examiner maps

[2] Lee et al., US 2013/0086309 A1 (pub. Apr. 4, 2013).

Lee's non-volatile dual in-line memory module ("NVDIMM") controller 306 to the recited "dedicated interface," finding that NVDIMM controller 306 is only available for communication between flash memory 302 and DRAM 304. Ans. 4–5 (citing Lee ¶ 86, Fig. 3A).

Appellant argues that the Examiner's interpretation of the recited "dedicated interface" to encompass Lee's memory controller is unreasonable because one of ordinary skill in the art would have understood the "distinction between a controller that manages data transfer (e.g., memory controller of Lee) relative to the interface upon which the data transfer occurs." Appeal Br. 5 (citing Spec. ¶¶ 16–17, 20–22); *see also* Reply Br. 3. Appellant further argues that "controller 306 of Lee . . . is explicitly communicable with the [memory controller hub ("MCH")] and thus communicates with components other than the DRAM and flash memory," and that, accordingly, NVDIMM controller 306 is not "only available for communication between the flash memory and the DRAM" as claimed. Appeal Br. 6; *see also* Reply Br. 3–4.

We agree with Appellant that the Examiner has erred. Lee's NVDIMM controller 306 "control[s] the NVDIMM DRAM and Flash memory operations" and "monitors events or commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH," but is not shown to be an interface through which data is transferred between the DRAM and flash memory. Lee ¶ 86; *see id.* Figs. 3A–B. Indeed, Figure 3A of Lee, cited by the Examiner, shows only one-way arrows from NVDIMM controller 306 to flash memory 302 and DRAM 304, indicating communication from NVDIMM controller 306 to each of flash memory 302 and DRAM 304, not

communication between flash memory 302 and DRAM 304 through NVDIMM controller 306.[3] Accordingly, we agree with Appellant that Lee's controller is not an "interface . . . for communication between the flash memory and the DRAM" (*see* Appeal Br. 5), let alone a "dedicated" interface "only available for communication between the flash memory and the DRAM," as claimed (*see id.* at 5–6; Reply Br. 3–4). As Appellant points out, Lee's NVDIMM controller 306 communicates with the MCH, as well as with flash memory 302 and DRAM 304. Lee ¶ 86 ("An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH)."), Fig. 3A; *see* Appeal Br. 5–6, Reply Br. 3–4.

Accordingly, on the record before us, we are constrained to reverse the Examiner's rejection of independent claims 21, 27, and 35, and, for the same reasons, claims 22–26, 28–34, and 36–40, which depend from them. Our reversal should not be taken as an indication of allowability. Whether the claimed subject matter is anticipated or would have been obvious to a person of ordinary skill in the art in view of any additional structure disclosed in Lee but not expressly relied upon by the Examiner is not a question before us, and we will not speculate in that regard here in the first instance on appeal.

[3] Other figures of Lee cited by the Examiner and corresponding disclosure similarly show that, while the memory controller manages data transfer between the DRAM and flash memory, it does not serve as the interface for that data transfer. *See* Lee Figs. 4A–B, 5A–B, ¶¶ 87, 92–93.

CONCLUSION

We reverse the Examiner's rejection of claims 21–40 under 35 U.S.C. § 102(a)(1).

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference/ Basis	Affirmed	Reversed
21–40	102(a)(1)	Lee		21–40

REVERSED