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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JIE ZHOU and ARTHUR J. KALB

Appeal 2019-001733
Application 14/534,662
Technology Center 2800

Before LINDA M. GAUDETTE, BRIAN D. RANGE, and JANE E. INGLESE, *Administrative Patent Judges.*

GAUDETTE, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

The Appellant[2] appeals under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1–15, 17–26, 28, 29, 31, and 32.[3]

We REVERSE.

[1] This Decision includes citations to the following documents: Specification filed Nov. 6, 2014 ("Spec."); Final Office Action dated Dec. 15, 2017 ("Final"); Appeal Brief filed June 12, 2018 ("Appeal Br."); Examiner's Answer dated Oct. 24, 2018 ("Ans."); and Reply Brief filed Dec. 21, 2018 ("Reply Br.").

[2] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. The Appellant identifies the real party in interest as Analog Devices, Inc. Appeal Br. 3.

[3] We have jurisdiction under 35 U.S.C. § 6(b).

CLAIMED SUBJECT MATTER

The invention is directed to an apparatus and methods for reducing charge injection mismatch in electronic circuits. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. An apparatus that is programmable to compensate for charge injection mismatch arising from manufacturing variation, the apparatus comprising:
>
> a programmable memory configured to generate a first control signal;
>
> a switch bank configured to receive a first input signal at a first input terminal and a second input signal at a second input terminal, wherein the switch bank is further configured to generate a first output signal at a first output terminal and a second output signal at a second output terminal, wherein *the switch bank comprises a selection circuit* and a plurality of switches; and
>
> an electronic circuit including a first input configured to receive the first output signal from the switch bank and a second input configured to receive the second output signal from the switch bank, *wherein the selection circuit is configured to select a first portion of the plurality of switches for operation in a first switch group based on a* ***non-periodic*** *setting provided by the first control signal, wherein the selection circuit is further configured to select a second portion of the plurality of switches for operation in a second switch group based on the* ***non-periodic*** *setting provided by the first control signal*, wherein the first switch group is configured to operate in a first signal path between the first input terminal and the first output terminal of the switch bank, wherein the second switch group is configured to operate in a second signal path between the second input terminal and the second output terminal of the switch bank, and wherein the first switch group and the second switch group are controllable by a first clock signal.

Appeal Br. 26 (emphases added).

REJECTIONS

1. Claims 1–13, 17–26, 28, 29, 31, and 32 are rejected under 35 U.S.C. § 103 as unpatentable over Burt (US 8,072,262 B1, issued Dec. 6, 2011) in view of Liu (US 6,639,532 B1, issued Oct. 28, 2003).

2. Claims 14 and 15 are rejected under 35 U.S.C. § 103 as unpatentable over Burt in view of Liu and Lewicki (US 6,259,313 B1, issued July 10, 2001).

OPINION

As an initial matter, we note that the "Appellant invites the Board to rule that the Examiner's Answer was improper, that the required Appeal Conference was not held, and to issue an opinion or guidance further clarifying the requirements for an Examiner's Answer and Appeal Conference." Appeal Br. 14. We decline to address these arguments as they do not affect the merits of the appeal. *See* 37 C.F.R. § 41.31(a)(1); MPEP § 1201 ("The line of demarcation between appealable matters for the Board . . . and petitionable matters for the Director of the U.S. Patent and Trademark Office . . . should be carefully observed.").

Each of independent apparatus claims 1 and 29 requires a programmable memory configured to generate a control signal, and a switch bank comprising a selection circuit and a plurality of switches. Appeal Br. 26, 32 (Claims Appendix). Claims 1 and 29 further require that the selection circuit is configured to select, based on a *non-periodic* setting provided by the control signal, first and second portions of the plurality of switches for operation in respective first and second switch groups. *Id.* Independent method claim 17 requires a switch bank that comprises a plurality of switches and is electrically coupled to an electronic circuit. *Id.* at 30. Claim

17 requires a step of observing a charge injection mismatch of the electronic circuit for various switch bank *non-periodic* settings that comprise different combinations of the plurality of switches in a first switch group and in a second switch group. *Id.* Claim 17 further requires steps of choosing a switch configuration based on the observations of the charge injection mismatch, and storing data corresponding to the chosen switch setting in a programmable memory such that the electronic circuit operates using the selected *non-periodic* switch setting. *Id.*

The Appellant contends that the Examiner erred reversibly in finding that Burt discloses or suggests an apparatus and a method that utilize *non-periodic* settings as required by independent claims 1, 17, and 29. *See generally* Appeal Br. 14–16, 18–20, 23. The Appellants added the term "non-periodic" to the claims in an amendment filed August 17, 2017 ("August Amendment"), responsive to the Examiner's April 17, 2017, Non-Final Office Action rejecting the claims as obvious over the combination of Burt and Liu. In the August Amendment, the Appellant acknowledged that the term "non-periodic" does not appear explicitly in the Specification, but argued that written descriptive support was provided in the Figure 8 method, namely "block 404, in which data corresponding to the selected switch configuration is stored in a programmable memory such that the electronic circuit operates with the selected switch configuration" (Spec. ¶ 118). *See* August Amendment 13. Referring to an online version of the Merriam-Webster Dictionary, the Appellant argued that the term "setting" means to adjust or to fix to a desired position. *Id.* The Appellant argued that Burt's pre- and post-chopping stages require clock signals to operate. *Id.* at 14. The Appellant argued that a clock signal is never set, and, therefore, the claim

term "non-periodic setting" did not read on Burt's apparatus and method. *Id.* at 13. The Appellant further argued that because chopper circuits require clock signals to operate, the ordinary artisan would not have modified Burt, based on Liu, to drive Burt's pre- and post-chopping stages by a non-periodic setting from a memory, as such modification would have rendered these stages inoperable because chopper circuits require clock signals to operate. *Id.* at 14.

In response to the Appellant's August Amendment, the Examiner issued a Final Office Action, citing Burt column 8, lines 53–64, in support of a finding that Burt teaches a selection circuit configured to select switches for operation in first and second switch groups based on a non-periodic setting provided by a "first control signal (via control signals to [switches] 26 and 30 . . .)." Final 17. The cited disclosure in Burt describes, in connection with Figure 4, "chopping signal PH1 which controls switches 26-1, 26-4, 30-1, and 30-4, and . . . chopping signal PH2 which controls switches 26-2, 26-3, 30-2, and 30-3. PHl is a sub-harmonic of Phasel and PH2 is a sub-harmonic of Phase2." Burt 8:54–58.

The Appellant argues that Burt's disclosure at column 8, lines 54–58 means that chopping signals PH1 and PH2 are *periodic* signals that are synchronized to the *periodic* clock signals Phase1 and Phase2. Appeal Br. 19–20. The Appellant explains that

> Burt operates in a first mode (i.e., with PH1 high) for some amount of time over . . . which some amount of input bias current is present. Then, Burt switches to a second mode (i.e., with PH2 high) for the same amount of time over which an allegedly similar amount of input bias current is present, but with an "opposite polarity" (col. 9, line 3) such that bias current caused by mismatches is reduced.

Appeal Br. 14; *see* Burt 8:65–9:7. The Appellant further argues that modifying Burt's apparatus and method, based on Liu's disclosure, to use programmable memory to generate the control signals for switches 26 and 30, would transform signals PH1 and PH2 from periodic signals to static signals, rendering Burt's apparatus unsatisfactory for its intended purpose of reducing input current by periodic reconfiguration of the input chopper stage 8. Appeal Br. 21–22.

We agree with the Appellant that the Examiner fails to address these arguments sufficiently in the Answer. Rather, the Examiner's Response to Argument largely repeats the same statements made in the Final Office Action. *See* Reply Br. 5–13 (comparing the language in the Final and the Answer). These statements amount to a recitation of the claim language and general citations to Burt's disclosure, but fail to explain with sufficient specificity why the Appellant's detailed explanation of why Burt's apparatus and method do not utilize *non-periodic* settings is erroneous or otherwise unpersuasive. *See* Ans. 5–6; Reply Br. 11–12.

In sum, the Appellant has argued persuasively that the Examiner has not shown, by a preponderance of the evidence, that independent claims 1, 17, and 29 are unpatentable over the combination of Burt and Liu. Accordingly we do not sustain the rejection of claims 1, 17, and 29, or the rejections of dependent claims 2–15, 18–26, 28, 31, and 32.

CONCLUSION

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–13, 17–26, 28, 29, 31, 32	103	Burt, Liu		1–13, 17–26, 28, 29, 31, 32
14, 15	103	Burt, Liu, Lewicki		14, 15
Overall Outcome				1–15, 17–26, 28, 29, 31, 32

REVERSED