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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DHARANI KOTTE, AKSHAY MATHUR, CHAYAN BISWAS, BASKARAN KANNAN, and SUMANT K. PATRO

Appeal 2019-001622
Application 14/323,896
Technology Center 2100

Before MICHAEL M. BARRY, PHILLIP A. BENNETT, and IFTIKHAR AHMED, *Administrative Patent Judges*.

AHMED, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 1–15, 18–22, and 24–29, which are all of the claims pending in the application. Claims 16, 17, and 23 are cancelled. Appeal Br. 27, 28. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). According to Appellant, the real party in interest is SanDisk Technologies LLC. Appeal Br. 3.

TECHNOLOGY

The application relates "generally to memory systems, and in particular, to real-time I/O pattern recognition to enhance performance and endurance of a storage device." Spec. ¶ 2.

ILLUSTRATIVE CLAIM

Claim 1 is illustrative and reproduced below with certain limitations at issue emphasized:

1. A data processing method, comprising:

at a storage device:

receiving from a host a plurality of input/output (I/O) requests, the I/O requests specifying operations to be performed in a plurality of regions in a *logical address space of the host*; and

performing one or more operations for each region of the plurality of regions in the *logical address space of the host*, including:

maintaining, and storing in a region data structure in the storage device, a history of I/O request patterns in the region *in the logical address space of the host* for a predetermined time period, the maintained history of I/O request patterns in the region including a plurality of count values for the region, each count value corresponding to a different I/O request pattern, wherein the plurality of count values are determined by tracking at least two of the following types of I/O requests in the region: sequential write requests, unaligned write requests, write requests to write data of a size less than a predefined small-size threshold, and write requests to write data of a size greater than a predefined large-size threshold; and

using the history of I/O request patterns in the region in the *logical address space of the host* to adjust subsequent I/O processing in the region.

REJECTIONS

Claims 1, 2, 19, 22, 25, and 26 stand rejected under 35 U.S.C. § 103 as obvious over the combination of de la Iglesia (US 2010/0115206 A1; May 6, 2010) ("Iglesia") and Benhase (US 2014/0019707 A1; Jan. 16, 2014). Final Act. 2.

Claims 3, 9–11, 14, and 15 stand rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, and Ng (US 2013/0073784 A1; Mar. 21, 2013). Final Act. 12.

Claims 4 and 5 stand rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and Nagasaki (US 2014/0032837 A1; Jan. 30, 2014). Final Act. 14.

Claim 6 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and Haynes (US 2008/0201661 A1; Aug. 21, 2008). Final Act. 16.

Claim 7 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and Tsai (US 2011/0026159 A1; Feb. 3, 2011). Final Act. 17.

Claim 8 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and Singh (US 8,909,894 B1; Dec. 9, 2014). Final Act. 18.

Claim 12 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and de la Iglesia (US 8,832,384 B1; Sept. 9, 2014 ("Iglesia '384")). Final Act. 19.

Claim 13 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and Nellans (US 2014/0101389 A1; Apr. 10, 2014). Final Act. 20.

Claim 18 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, Ng, and de la Iglesia (US 8,775,741 B1; July 8, 2014) ("Iglesia '741"). Final Act. 20.

Claims 20 and 21 stand rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, and Loh (US 2014/0181458 A1; June 26, 2014). Final Act. 21.

Claim 24 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, and Iglesia '741. Final Act. 22.

Claims 27 and 28 stand rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, and Nagasaki. Final Act. 23.

Claim 29 stands rejected under 35 U.S.C. § 103 as obvious over the combination of Iglesia, Benhase, and Haynes. Final Act. 25.

ISSUE

Did the Examiner err in finding that Iglesia teaches or suggests a "logical address space of the host," as recited in claim 1?

ANALYSIS

Independent claim 1 recites performing and tracking operations for regions in the "logical address space of the host." The Examiner relies on Iglesia as teaching this limitation, finding that "Iglesia discloses . . . groups of blocks are logically grouped together into highly clustered address regions/areas 40 according to the previously monitored read and write access patterns by one or more clients 10." Ans. 26 (citing Iglesia ¶ 53, Figs. 1–4) (referring to "prefetch groups" 40 shown in Fig. 2). The Examiner notes that "[t]he sub-records [in Iglesia] include area reference identifiers 252 that identify the address regions 20," and "read/write operations can access the

address regions using th[ose] reference identifiers," thereby teaching the claimed logical address space. *Id.* (referring to historical records maintained in table 34 as shown in Iglesia Fig. 5) (citing Iglesia ¶ 54). Those prefetch groups, the Examiner concludes, teach the claimed regions in the logical address space of the host. *Id.* The Examiner reasons "[a]ccessing using an identifier is same as accessing using logical address since both are methods of accessing using an address/identifier to access data." *Id.* "Since read/write operations access storage regions using addresses in a subset," the Examiner concludes, Iglesia's teaching "is equivalent to the logical address space of the host." *Id.*

Appellant argues that Iglesia's "address regions are *physical address regions*, not regions in a logical address space of a host device or system." Appeal Br. 15 (citing Iglesia Figs. 4, 5). Appellant asserts that "address regions 40A-40Z refer to *physical address regions* (e.g., within disk memory blocks) of storage device 20," in Figures 4 and 5 of Iglesia. *Id.* at 15 (emphasis added). Appellant contends that Iglesia's reference to physical address regions is further confirmed by its use of phrases such as "address regions of contiguously accessed memory locations" and "storage address regions." *Id.* (citing Iglesia Abstract, ¶ 29). Appellant therefore argues that Iglesia does not teach or suggest "maintaining a history of I/O request patterns in the region *in the logical address space of the host*," as recited in claim 1. *Id.* at 17.

We agree with Appellant that the Examiner errs. The Examiner has not sufficiently explained how Iglesia teaches or suggests a "logical address space of the host." Although Iglesia teaches groups of blocks in a storage device that are logically grouped together, and that each block has a starting

block address and an ending block address, there is no indication that these blocks relate to the *logical* address space of the host. These blocks are clearly identified by their *physical* addresses, as can be seen from Figures 4 and 5 of Iglesia — the collection of memory blocks shown in Figure 4 is labeled as a "disk." As Iglesia makes clear, the storage device disclosed in Iglesia is "viewed as a large contiguous range of blocks," and access operations to the device are through physical addresses, expressed as a number of blocks:

> The address is often expressed in *terms of blocks* (such as a read of *blocks 100-200*) where storage device 20 is viewed as a large *contiguous range of blocks*. The length of the storage device access operation is similarly expressed as a number of blocks. Thus, every read or write from client 10 to storage device 20 can be viewed as affecting a *block range* (from address to address plus length).

Iglesia ¶ 30 (emphasis added).

The prefetch groups in Iglesia that the Examiner relies on as a logical address space are *created* by the prefetch controller *based on* "read or write operation performed by the client 10 with storage device 20." *Id.* ¶¶ 37, 38. "Prefetching is a caching technique used for improving the performance of disk" by "effectively guessing what future data accesses will be." *Id.* ¶¶ 2, 8. Iglesia's prefetch controller implements this technique by "aggregat[ing] the events 30 into contiguous prefetch groups/address ranges 40," i.e., it creates logical groups of *physical* blocks that have been accessed by the client over a given period of time. *Id.* ¶¶ 38–41, Fig. 2 (providing examples). Iglesia uses these groups to determine what data to *load into cache memory* (using physical addresses) when it receives a subsequent client request. *Id.* ¶ 51 (referring to memory blocks that are cached). The

reference identifiers that the Examiner relies on as disclosing logical addresses (Ans. 26) are used by Iglesia to determine the sequence of physical addresses for prefetch groups to be loaded into the cache memory. Iglesia ¶ 80, Fig. 8. The prefetch groups therefore are not regions in a logical address space, and Iglesia does not disclose using logical addresses to perform host access operations.

Independent claim 1, however, requires performing operations for regions in "the logical address space of the host," which is different from the physical address ranges of a storage device. *See* Spec. ¶¶ 64, 67, Fig. 4. The record before us, therefore, does *not* demonstrate that Iglesia teaches or suggests a "logical address space of the host," as recited in claim 1. The Examiner also does not rely on Benhase as meeting this claim limitation in support of the obviousness rejection based on Iglesia and Benhase.

Accordingly, on the record before us, we do not sustain the Examiner's rejection of independent claims 1, 22, and 25, and their dependent claims 2–15, 18–21, 24, and 26–29.

DECISION

For the reasons above, we reverse the Examiner's decision rejecting claims 1–15, 18–22, and 24–29.

In summary:

Claims Rejected	Statute	References	Affirmed	Reversed
1, 2, 19, 22, 25, 26	§ 103	Iglesia, Benhase		1, 2, 19, 22, 25, 26
3, 9–11, 14, 15	§ 103	Iglesia, Benhase, Ng		3, 9–11, 14, 15
4, 5	§ 103	Iglesia, Benhase, Ng, Nagasaki		4, 5
6	§ 103	Iglesia, Benhase, Ng, Haynes		6
7	§ 103	Iglesia, Benhase, Ng, Tsai		7
8	§ 103	Iglesia, Benhase, Ng, Singh		8
12	§ 103	Iglesia, Benhase, Ng, Iglesia ’384		12
13	§ 103	Iglesia, Benhase, Ng, Nellans		13
18	§ 103	Iglesia, Benhase, Ng, Iglesia ’741		18
20, 21	§ 103	Iglesia, Benhase, Loh		20, 21
24	§ 103	Iglesia, Benhase, Iglesia ’741		24
27, 28	§ 103	Iglesia, Benhase, Nagasaki		27, 28
29	§ 103	Iglesia, Benhase, Haynes		29
Overall Outcome				1–15, 18–22, 24–29

REVERSED