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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/777,787	02/26/2013	James J. Fitzgibbon	5569-98843-US	9907

150733 7590 08/18/2020

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ART UNIT	PAPER NUMBER
2437	

MAIL DATE	DELIVERY MODE
08/18/2020	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES J. FITZGIBBON and ERIC GREGORI

Appeal 2019-001132
Application 13/777,787
Technology Center 2400

Before THU A. DANG, ELENI MANTIS MERCADER, and BETH Z. SHAW, *Administrative Patent Judges.*

MANTIS MERCADER, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1, 2, 5–9, 14–18, and 26–30. *See* Final Act. 1. We have jurisdiction under 35 U.S.C. § 6(b).

We conducted an oral hearing for this case on August 4, 2020.

We REVERSE.

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[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as The Chamberlain Group, Inc. Appeal Br. 3.

CLAIMED SUBJECT MATTER

The claims are directed to a transmission of data including conversion of ternary data to binary data. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method comprising:
>
> preparing for transmission of data between a movable barrier operator and a peripheral device by:
>
> converting first binary data comprising information relating to the movable barrier operator into ternary data using a first conversion method;
>
> converting the ternary data to a binary format to provide binary information representative of the information relating to the movable barrier operator, the converting done in a way not mirroring the first conversion method;
>
> transmitting the binary information between the movable barrier operator and the peripheral device including transmitting pairs of binary bits wherein at least one of the pairs of binary bits represents a particular ternary value and a different one of the pairs of binary bits represents an illegal value;
>
> receiving by one of the movable barrier operator and the peripheral device at least one pair of binary bits representing the illegal value to effect synchronization of communication between the movable barrier operator and the peripheral device by using the illegal value as a marker for starting or ending reading the binary information.

REFERENCES

The prior art relied upon by the Examiner is:

Name	**Reference**	**Date**
Warner	US 4,243,976	Jan. 6, 1981
Farris	US 2002/0034303 A1	Mar. 21, 2002

REJECTION

Claims 1, 2, 5–9, 14–18, and 26–30 stand rejected under

35 U.S.C. § 103(a) as being unpatentable over Farris in view of Warner.

Claims Rejected	35 U.S.C. §	Reference(s)/Basis
1, 2, 5–9, 14–18, 26–30	103	Farris in view of Warner

OPINION

Claims 1, 2, 5–9, 14–18, and 26–30 stand rejected under 35 U.S.C. § 103(a)

Appellant argues *inter alia* that neither Farris nor Warner alone or in combination teach or suggest the limitation of "transmitting pairs of binary bits wherein at least one of the pairs of binary bits represents a particular ternary value and a different one of the pairs of binary bits represents an illegal value" as recited in claim 1. *See* Appeal Br. 8.

Appellant acknowledges that Farris teaches converting data from binary to ternary and transmitting ternary coded information. Appeal Br. 8 (citing Farris para. 10). Appellant further acknowledges that Farris teaches ternary coded information preceded by a "single synchronization and/or identification pulse." *Id.* (citing Farris para. 11). Appellant cites to Farris for teaching a synchronization pulse of a particular timing duration at the start of a frame. *Id.* (citing SYNC 0.5 and SYNC 1.5 in the pulse trains illustrated in Farris's FIG. 6).

However, Appellant argues that Farris's "single synchronization and/or identification pulse" does not meet the claim limitation of being a "pair of binary bits," which is defined by Appellant's Specification as: "[a] pair of binary bits can represent 4 discrete information elements." Appeal Br. 8 (citing Spec. paras. 28, 46–47 and FIG. 6). Appellant notes that the Specification uses a common understanding of the terms "binary" and "bit"

where binary means having two states and bit is a representation of information. *Id.* at 8–9.

The Examiner finds that the sync pulses will be identified following a predetermined inactive period. Ans. 3 (citing Farris paras. 11, 33, Fig. 6, BLANK). According to the Examiner after the inactive period has expired, a 0.5 millisecond up signal will identify the first 20-trinary bit frame and a 1.5 millisecond up signal will identify the second 20-trinary bit frame. *Id.* (citing Farris' para. 33 and Fig. 6). The Examiner concludes that Farris teaches the transmission of a pair of binary bits because the inactive period would represent a 0 binary bit and the 0.5 millisecond up signal or the 1.5 millisecond up signal would represent a 1 binary bit. *Id.* According to the Examiner, this pair of binary bits transmitted by Farris would represent "an illegal value" as claimed because it acts as a sync pulse to identify bit frames constituting a single synchronization and/or identification pulse indicating the start of the frame and whether it is the first frame or the second frame which is consistent with the "illegal value" being used as a marker for starting or ending reading of the binary information. *Id.* at 3–4 (citing Farris paras. 11 and 33).

"During examination, 'claims . . . are to be given their broadest reasonable interpretation consistent with the specification, and . . . claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.'" *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citation omitted). We turn to Appellant's Specification to ascertain the meaning of the term "illegal value."

Figure 6 reproduced below shows the ternary data element "0" (which corresponds to the usual binary data element "0") mapping to the binary pair

"00," ternary "1" corresponding to usual binary "1" mapping to the binary pair "01" and ternary "2" which corresponds to usual binary "11" mapping to the binary pair "1." *See* Spec. para. 46.

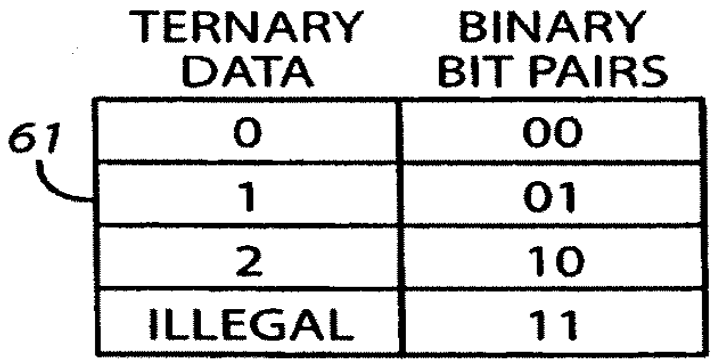

FIG. 6

Figure 6 shows the ternary data to binary bit pairs conversion and the "illegal value" binary bit pair.

Appellant's Specification discloses in paragraphs 46 and 47 in reference to Figure 6 reproduced below the following:

> [0046] . . . FIG. 6, the ternary data element "0" (which corresponds to the usual binary data element "0") maps to the binary pair "00." In similar fashion, ternary "1" (which corresponds to usual binary "1") maps to the binary pair "01" and ternary "2" (which corresponds to usual binary "11") maps to the binary pair "01."
>
> [0047] This leaves an otherwise unused binary pair "11." Pursuant to a preferred approach, this otherwise illegal value can serve a synchronization function when facilitating communications as between a movable barrier operator and one or more peripheral components when using a binary format that

> otherwise has no synchronization mechanism built into its format (for example, a stream of binary bits such as:
>
> 011011111110100111011101101111111010011101110110111111101001110111
>
> which format lacks a frame marker or other point of synchronization). To illustrate, a synchronization signal/marker comprising this "11" binary pair can be used to indicate, for example, the regular end and/or start of a frame or message as in the following example:
>
> **11**011011111101*11*10111011**11**011011111101*11*1110111**11**1 10110111111101*11*11
> where the bold font "11" regularly spaced binary pairs serve as frame markers (and which, due to their synchronized regular spacing, are readily distinguishable from other "11" pairs as may occur for whatever reason (illustratively depicted in the above example with italic font).

Spec. paras. 46, 47.

We agree with Appellant that the Examiner's clarification in the Answer finding the dead time between pulses as logic "0" and the SYNC pulse corresponding to logic "l" is in error. *See* Reply Br. 2 (citing Ans. 3). We agree with Appellant that the dead time in Farris is not logic "0." *See id.*

Farris defines logic "0" as follows: "the bit timing in FIG. 6 for a 0 is 1.5 milliseconds down time and 0.5 millisecond up time." Reply Br. 2 (citing Farris para. 32). We also agree with Appellant that Farris never refers to the dead time between transmission frames as being considered a logic "0." *Id.*

We further agree with Appellant that the Specification defines "illegal value" as an otherwise unused binary pair when mapping pairs of binary elements to ternary logic values. Reply Br. 2 (citing Spec. paras. 47,

53). We agree with Appellant that the Examiner's Answer does not address how Farris's pulses that are understood per the Examiner's analysis to be logic "0" and "1" constitute an "illegal value" as claimed in light of Appellant's Specification. *See id.*

Warner does not cure the above cited deficiencies. Accordingly, we reverse the Examiner's rejection of claims 1, 2, 5–9, 14–18, and 26–30 over the combination of Farris and Warner.

CONCLUSION

The Examiner's rejection is REVERSED.

More specifically, the Examiner's rejection of claims 1, 2, 5–9, 14–18, and 26–30 under 35 U.S.C. § 103(a) is reversed.

DECISION SUMMARY

Claims Rejected	**35 U.S.C. §**	**Reference(s)/Basis**	**Affirmed**	**Reversed**
1, 2, 5–9, 14–18, 26–30	103	Farris, Warner		1, 2, 5–9, 14–18, 26–30

REVERSED