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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ANDREAS HANSSON and IAN RUDOLF BRATT

Appeal 2019-001091
Application 14/969,414
Technology Center 2100

Before JEREMY J. CURCURI, BARBARA A. BENOIT, and SCOTT RAEVSKY, *Administrative Patent Judges*.

CURCURI, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM IN PART.

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[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as ARM Limited. Appeal Br. 3.

CLAIMED SUBJECT MATTER

The claims are directed to "issuing access requests to a memory controller." Spec. 2:2–3. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A requesting agent device, comprising:
>
> a request interface to issue access requests from the requesting agent device to a memory controller for a memory device whose memory structure consists of a plurality of sub-structures, each access request identifying a memory address;
>
> an abstraction data storage to store static abstraction data providing an indication of one or more of the sub-structures;
>
> an outstanding access requests storage to store an indication of outstanding access requests issued from the request interface; and
>
> next access request selection circuitry to select from a plurality of candidate access requests a next access request for issuance from the request interface to the memory controller, said selection being dependent on sub-structure indication data derived from application of an abstraction data function, using said static abstraction data, to the memory addresses of the candidate access requests and the outstanding access requests.

REFERENCES

The prior art relied upon by the Examiner is:

Name	Reference	Date
LeClerg	US 6,857,041 B2	Feb. 15, 2005
Moscibroda	US 2009/0055580 A1	Feb. 26, 2009
Resnick	US 2009/0150624 A1	June 11, 2009
Warshofsky	US 8,019,950 B1	Sept. 13, 2011

REJECTIONS

Claims 1–5, 7, and 15–20 are rejected under 35 U.S.C. §§ 102(a)(1) and 102(a)(2) as anticipated by Resnick. Final Act. 2–7.

Claim 6 is rejected under 35 U.S.C. § 103 as obvious over Resnick and Warshofsky. Final Act. 8–9.

Claims 8–12 are rejected under 35 U.S.C. § 103 as obvious over Resnick, Warshofsky, and Moscibroda. Final Act. 9–16.

Claims 13 and 14 are rejected under 35 U.S.C. § 103 as obvious over Resnick and LeClerg. Final Act. 16–17.

OPINION

The Anticipation Rejection of Claims 1–5, 7, and 15–20 by Resnick

The Examiner finds Resnick describes all limitations of claim 1. Final Act. 2–4; *see also* Ans. 3–7. The Examiner finds Resnick (Resnick, Fig. 1, requesters 230, request bus 240) discloses "a request interface" as recited in claim 1. Final Act. 2–3. The Examiner finds Resnick (Resnick, Fig. 2, request queue 110) discloses "an abstraction data storage" as recited in claim 1. Final Act. 3. The Examiner finds Resnick (Resnick, Fig. 2, bank queues 130) discloses "an outstanding access requests storage" as recited in claim 1. Final Act. 3. The Examiner finds Resnick (Resnick, Fig. 2, ordering unit 140) discloses "next access request selection circuitry" as recited in claim 1. Final Act. 3–4.

Put another way, the Examiner finds the claimed "requesting agent device" (claim 1, preamble) corresponds to Resnick's requesters 230 and request bus 240, and various structures in Resnick that are part of Resnick's memory controller 100 (Resnick, Figs. 1 and 2). *See* Final Act 2 (citing Resnick ¶ 22); *see also* Ans. 7 ("When the request queue component, bank

queue components, and ordering unit component [are] integrated into Resnick's requester #230, the memory controller itself would still include at least the data buffer #150, memory interface #160 and timing controller #170 (see Figure 2 of Resnick).").

Appellant presents the following principal argument:

Resnick does not disclose the claimed "requesting agent device" (claim 1, preamble) because, for findings directed to various recited claim elements, the Examiner cites to structures in Resnick that are part of Resnick's memory controller (Resnick, Figs. 1 and 2, memory controller 100), and "[n]o reasonable interpretation of the claimed requesting agent [device] understood in light of and consistent with the specification would encompass functionality and components in a memory controller." Appeal Br. 8; *see also* Appeal Br. 10 ("[T]he claimed requesting agent device logically should be mapped to Resnick's actual requesting agent 230/225."), 13 ("The language 'memory controller' recited in claim 1 can only reasonably be mapped to Resnick's 'memory controller 100' shown in Figure 1."), 15 ("While Resnick's *memory controller* 100 selects which access request to process next from the requests that have been received by the memory controller, the claimed *requesting agent device* seeks to optimize the order in which requests are sent to the memory controller.").

Regarding *integration* of memory controller components into the requestor of Resnick (*see* Ans. 7), in the Reply Brief in response to the Examiner's Answer, Appellant argues "[t]hose three additions from the memory controller 100 [in Resnick] to the requester 230 [in Resnick] are made entirely by the Examiner—not by Resnick." Reply Br. 3.

We do not see any reversible error in the contested findings of the Examiner. We concur with the Examiner's conclusion of anticipation.

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted) (internal quotation marks omitted). Additionally, "[t]hough understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim." *See SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

We determine that the broadest reasonable interpretation of claim 1 encompasses any arrangement that includes structures corresponding to each recited element and for performing each recited function because the "requesting agent device" (claim 1, preamble) recites various structures for performing various functions, and is defined only by these recited structures and functions and not by Appellant's Specification and Figures. *See* Ans. 3 ("[T]he claimed requesting agent device is defined by its functionality and not the name.").

Thus, we agree with and adopt as our own the Examiners findings that Resnick (Resnick, Fig. 1, requesters 230, request bus 240) discloses "a request interface" as recited in claim 1, Resnick (Resnick, Fig. 2, request queue 110) discloses "an abstraction data storage" as recited in claim 1, Resnick (Resnick, Fig. 2, bank queues 130) discloses "an outstanding access requests storage" as recited in claim 1, and Resnick (Resnick, Fig. 2, ordering unit 140) discloses "next access request selection circuitry" as recited in claim 1. Final Act. 2–4.

In adopting these findings, we do not need to determine whether or not Resnick (Resnick ¶ 22) discloses integration of memory controller

components from memory controller 100 into the requester 230 of Resnick because our interpretation of claim 1 does not require integration of all the components from Resnick's memory controller 100, depicted in Figure 2, into the requester 230 of Resnick. Rather, we determine claim 1 encompasses any arrangement that includes structures corresponding to each recited element and for performing each recited function, such as the arrangement in Resnick presented by the requester 230 and memory controller 100.

Further, regarding claim 1's requirement that access requests are issued "to a memory controller," the arrangement in Resnick also meets this requirement. We determine that the broadest reasonable interpretation of the recited "memory controller" includes its plain meaning, which is a device that controls memory. That is, the claimed "memory controller" includes Resnick's memory interface 160 because, under the broadest reasonable interpretation, memory interface 160 provides memory control and address signals on memory control bus 172. *See* Resnick, Figure 2; *see also* Ans. 7. Again, claim 1 does not require integration of all the memory controller components depicted in Resnick's Figure 2 memory controller 100 into the requester 230 of Resnick. In other words, even though Resnick describes the entire structure of Figure 2 as a memory controller in one embodiment, we find that under the broadest reasonable interpretation, the memory interface 160 alone is also a memory controller.

We, therefore, sustain the Examiner's rejection of claim 1.

We also sustain the Examiner's rejection of claims 2–5, 7, and 15–20, which are not separately argued with particularity. *See* Appeal Br. 16–17; *see also* Reply Br. 4–5.

Regarding claim 3, claim 3 further recites "wherein said at least a subset of said outstanding access requests comprises all outstanding access requests indicated in said outstanding access requests storage."

The Examiner finds Resnick describes the further recited subject matter of claim 3. Final Act. 5 (citing Resnick ¶ 29); *see also* Ans. 8. Resnick discloses "[t]he ordering unit 140 tracks the information in the bank queues 130 and indicates to the memory interface 160 and timing controller 170 the order in which memory requests should be taken from the bank queues 130 and which bank queue 130 should supply the next memory access request." Resnick ¶ 29.

Appellant argues "Resnick does not disclose that requesting agent device 230 has access to the claimed an indication of the memory sub-structures. This makes sense because this access would be handled by Resnick's memory controller 100." Appeal Br. 16.

Appellant further argues regarding comparison data for "*all* outstanding access requests" (emphasis added) as recited in claim 3, "[a]ll outstanding requests [in Resnick] includes requests in the bank queues 130 other than the queue to which that incoming request will be allocated." Appeal Br. 16; *see also* Reply Br. 4–5.

We do not see any reversible error in the contested findings of the Examiner. We concur with the Examiner's conclusion of anticipation.

Regarding Appellant's first argument, as we explained above when addressing claim 1, the claimed "memory controller" corresponds to Resnick's memory interface 160 (Resnick, Fig. 2). *See* Ans. 7. Further, the claimed "requesting agent device" corresponds to Resnick's requesters 230, request bus 240, request queue 110, bank queues 130, and ordering unit 140 (Resnick, Figs. 1 and 2). *See* Final Act. 2–4. Thus, we do not need to

determine whether or not Resnick's requesters 230 have access to an indication of the memory sub-structures.

Regarding Appellant's second argument and comparison data for "*all* outstanding access requests" (emphasis added) as recited in claim 3, we do not need to determine whether or not Resnick considers requests in *all* bank queues because a skilled artisan would have understood that Resnick's memory subsystem may include only a single bank. Further, Resnick's ordering unit indicates "the order in which memory requests should be taken from the bank queues 130 *and which bank queue 130 should supply the next memory access request*." Resnick ¶ 29 (emphasis added). Thus, Resnick considers requests in *all* bank queues, and describes the further recited subject matter of claim 3.

We, therefore, sustain the Examiner's rejection of claim 3.

Regarding claim 19, claim 19 further recites "wherein the requesting agent device comprises on-chip memory interface circuitry of an integrated circuit, and *the memory controller is off-chip*" (emphasis added).

The Examiner finds Resnick describes the further recited subject matter of claim 19. Final Act. 7 (citing Resnick ¶ 22); *see also* Ans. 8 ("Resnick's request queue, bank queues and ordering unit[] are integrated into the requester unit.").

Appellant argues "[t]he Examiner's improper interpretation relies on the requesting device and memory controller being integrated in the same integrated circuit, which is clearly not possible for claim 19." Appeal Br. 17; *see also* Reply Br. 5.

We have reviewed the arguments and evidence, and we determine the Examiner erred in finding Resnick describes the further recited subject matter of claim 19.

Resnick discloses

> In addition, the bridge unit 250 may be configured with the memory controller 100 and the bus bridge 260 as separate devices or the bridge unit 250 may integrate the memory controller 100 and the bus bridge 260 into a single device. In addition, the bridge unit 250, or the separate components of the memory controller 100 and bus bridge 260, may be integrated in the same packages or integrated circuits as the requestor units 230.

Resnick ¶ 22.

We interpret Resnick as disclosing integrating the bridge unit 250 into the requestor units 230, and the bridge unit itself may be composed of separate devices or a single integrated device. We do not interpret Resnick as disclosing integrating only certain individual components of memory controller 100 into the requestor units 230. Thus, Resnick does not describe "the requesting agent device comprises on-chip memory interface circuitry of an integrated circuit, and *the memory controller is off-chip*" (emphasis added) as recited in claim 19.

We, therefore, do not sustain the Examiner's rejection of claim 19.

The Obviousness Rejection of Claim 6 over Resnick and Warshofsky

Appellant does not present any separate argument with respect to claim 6. *See* Appeal Br. 16–17; *see also* Reply Br. 4–5.

We, therefore, sustain the Examiner's rejection of claim 6 for the same reasons discussed above when addressing claim 1.

The Obviousness Rejection of Claims 8–12 over Resnick, Warshofsky, and Moscibroda

Appellant does not present any separate argument with respect to claims 8–12. *See* Appeal Br. 16–17; *see also* Reply Br. 4–5.

We, therefore, sustain the Examiner's rejection of claims 8–12 for the same reasons discussed above when addressing claim 1.

The Obviousness Rejection of Claims 13 and 14 over Resnick and LeClerg

Appellant does not present any separate argument with respect to claims 13 and 14. *See* Appeal Br. 16–17; *see also* Reply Br. 4–5.

We, therefore, sustain the Examiner's rejection of claims 13 and 14 for the same reasons discussed above when addressing claim 1.

CONCLUSION

The Examiner's decision to reject claims 1–18 and 20 is affirmed.

The Examiner's decision to reject claim 19 is reversed.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–5, 7, 15–20	102	Resnick	1–5, 7, 15–18, 20	19
6	103	Resnick, Warshofsky	6	
8–12	103	Resnick, Warshofsky, Moscibroda	8–12	
13, 14	103	Resnick, LeClerg	13, 14	
Overall Outcome			**1–18, 20**	**19**

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED IN PART