UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/391,470	12/27/2016	Scott Hilker	1458-100536DIV2	8320

109712 7590 12/16/2019

Advanced Micro Devices, Inc.
c/o Davidson Sheehan LLP
6836 Austin Center Blvd.
Suite 320
Austin, TX 78731

EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
12/16/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

AMD@DS-patent.com
docketing@ds-patent.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SCOTT HILKER

Appeal 2019-000318
Application 15/391,470
Technology Center 2100

BEFORE KRISTEN L. DROESCH, JAMES W. DEJMEK, and STEPHEN E. BELISLE, *Administrative Patent Judges*.

DROESCH, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 8–13, all of the pending claims.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

---

[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a) (2017). Appellant identifies the real party in interest as Advanced Micro Devices, Inc. Appeal Br. 1.

[2] Claims 1–7 and 14–20 have been cancelled.

CLAIMED SUBJECT MATTER

The disclosed invention relates to processors and processing circuits, in particular, a method for a floating point multiply accumulator (FMAC) multi-precision mantissa aligner. Spec. 2:6–8. Claim 8, reproduced below, is illustrative of the claimed subject matter:

> 8. A method comprising:
> multiplying, at a floating point multiply accumulator, a first binary number and a second binary number to obtain a product, wherein multiplying comprises adding a first exponent value associated with the first binary number to a second exponent value associated with the second binary number to obtain an exponent sum and multiplying a first mantissa value associated with the first binary number to a second mantissa value associated with the second binary number, and wherein the exponent adding and the mantissa multiplying are performed substantially in parallel; and
> performing, at the floating point multiply accumulator, at least one of adding a third binary number to the product or subtracting the third binary number from the product.

REJECTION

Claims 8–13 stand rejected under 35 U.S.C. § 101 as directed to patent-ineligible subject matter.

OPINION

Appellant disputes the Examiner's conclusion that claims 8–13 are directed to patent-ineligible subject matter. *See* Appeal Br. 2–5; Reply Br. 2–3. Appellant argues claims 8–13 together as a group. *See* Appeal Br. 2–5; Reply Br. 2–3. Consequently, we choose claim 8 as representative of the group. 37 C.F.R. § 41.37(c)(1)(iv). In particular, Appellant contends that the Examiner erred because the claims are not directed to an abstract idea. *See* Appeal Br. 3. According to Appellant, *Enfish LLC v. Microsoft*

Corp., 822 F.3d 1327 (Fed. Cir. 2016) holds that claims directed to an improvement in the operation of an electronic device, such as a computer, are not abstract ideas, and, therefore, patent eligible under § 101. *See id.* at 3, 5. Appellant argues claim 8 is tied to a machine—a floating point multiply accumulator (FMAC) and claims 8–13 are directed to improvements in the operation of the FMAC. *See* Appeal Br. 3–4 (citing Spec. 6:7–23, 12:1–17). Appellant contends that the claimed techniques improve the operation of the computer itself, because the claimed techniques support mantissa alignment which can lead to power saving, decreased latency, and increased throughput. *See id.* Appellant further argues the Office failed to establish a prima facie case that the claims are directed to a judicial exception because the Office has merely asserted the claims are abstract. *See id.* at 4–5. Appellant contends that because the Examiner has provided no evidence or argument that the claims are not directed to an improvement in the operation of an FMAC, the Examiner's conclusory statements cannot establish that claim 8 is abstract. *See id.* at 5.

The Supreme Court's two-step framework guides our analysis of patent eligibility under 35 U.S.C. § 101. *Alice Corp. v. CLS Bank Int'l*, 573 U.S. 208, 217 (2014). In addition, the Office recently published revised guidance for evaluating subject matter eligibility under 35 U.S.C. § 101, specifically with respect to applying the *Alice* framework. USPTO, *2019 Revised Patent Subject Matter Eligibility Guidance*, 84 Fed. Reg. 50 (Jan. 7, 2019) ("Guidance"). If a claim falls within one of the statutory categories of patent eligibility (i.e., a process, machine, manufacture, or composition of matter) then the first inquiry is whether the claim is directed to one of the judicially recognized exceptions (i.e., a law of nature, a natural phenomenon,

or an abstract idea). *Alice*, 573 U.S. at 217. As part of this inquiry, we must "look at the 'focus of the claimed advance over the prior art' to determine if the claim's 'character as a whole' is directed to excluded subject matter." *Affinity Labs of Tex., LLC v. DIRECTV, LLC*, 838 F.3d 1253, 1257 (Fed. Cir. 2016). According to the recent Guidance, this first inquiry has two prongs of analysis (i) does the claim recite a judicial exception (e.g., an abstract idea); and (ii) if so, is the judicial exception integrated into a practical application. *See* Guidance, 84 Fed. Reg. at 54. Under the Guidance, if the judicial exception is integrated into a practical application, the claim is patent eligible under § 101. *See id.* at 54–55. If the claims are not directed to a judicial exception, the inquiry ends. *See McRO, Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299, 1312 (Fed. Cir. 2016). However, if the claim *is* directed to a judicial exception (i.e., recites a judicial exception and does not integrate the exception into a practical application), the next step is to determine whether any element, or combination of elements, amounts to significantly more than the judicial exception itself. *See Alice*, 573 U.S. at 217; *see also* Guidance, 84 Fed. Reg. at 56.

Here, we conclude that claim 8 generally recites multiplying first and second binary numbers to obtain a product by, in parallel, adding exponent values and multiplying mantissa values of the first and secondary binary numbers, and then adding a third binary number to the product and/or subtracting the third binary number from the product. This is consistent with how Appellant describes the claimed invention. *See* Spec. 3:6–14, 12:1–17; Fig. 5.

Consistent with the Guidance and case law, we conclude that multiplying first and second binary numbers to obtain a product by, in parallel, adding exponent values and multiplying mantissa values of the first and secondary binary numbers, and then adding a third binary number to the product and/or subtracting the third binary number from the product are mathematical calculations—a mathematical concept, and, thus, an abstract idea. *See* Guidance, 84 Fed. Reg. at 52; *SAP America, Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1163 (Fed. Cir. 2018); *RecogniCorp, LLC v. Nintendo Co.*, 855 F.3d 1322, 1326–27 (Fed. Cir. 2017); *Digitech Image Techs., LLC v. Electronics for Imaging, Inc.*, 758 F.3d 1344 (Fed. Cir. 2014); *Bilski v. Kappos*, 561 U.S. 593, 611 (2010); *Diamond v. Diehr*, 450 U.S. 175, 191 (1981); *Parker v. Flook*, 437 U.S. 584, 594 (1978); *Gottschalk v. Benson*, 409 U.S. 63, 71–72 (1972).

Claim 8 is reproduced below and includes the following claim limitations that recite mathematical calculations, emphasized in *italics*:

> 8. A method comprising:
> *multiplying*, at a floating point multiply accumulator, *a first binary number and a second binary number to obtain a product, wherein multiplying comprises adding a first exponent value associated with the first binary number to a second exponent value associated with the second binary number to obtain an exponent sum and multiplying a first mantissa value associated with the first binary number to a second mantissa value associated with the second binary number, and wherein the exponent adding and the mantissa multiplying are performed substantially in parallel*; and
> *performing*, at the floating point multiply accumulator, *at least one of adding a third binary number to the product or subtracting the third binary number from the product*.

Because the claim recites a judicial exception, we next determine whether the claim integrates the judicial exception into a practical

application. *See* Guidance, 84 Fed. Reg. at 54. To determine whether the judicial exception is integrated into a practical application, we identify whether there are "*any additional elements recited in the claim beyond the judicial exception(s)*" and evaluate those elements to determine whether they integrate the judicial exception into a recognized practical application. Guidance, 84 Fed. Reg. at 54–55 (emphasis added); *see* Manual of Patent Examining Procedure ("MPEP") § 2106.05(a)–(c), (e)–(h) (9th ed. Rev. 08.2017, Jan. 2018).

Here, we find the additional limitations do not integrate the judicial exception into a practical application. Although Appellant asserts that the claims are directed to an improvement in the operation of an electronic or computer device (*see* Appeal Br. 3–5), the claims do not recite an improvement to the functionality of a computer or other technology or technical field (*see* MPEP § 2106.05(a)). The claims also do not recite: (i) a "particular machine" to apply or use the judicial exception (*see* MPEP § 2106.05(b)); (ii) a particular transformation of an article to a different thing or state (*see* MPEP § 2106.05(c)); or (iii) any other meaningful limitation (*see* MPEP § 2106.05(e)). *See* Guidance, 84 Fed. Reg. at 55.

The only additional limitation of claim 8 is "at a floating point multiply accumulator." We agree with the Examiner that the mathematical calculations recited in claim 8 can be performed by a generic processor. *See* Ans. 4; Final Act. 4. Moreover, Appellant acknowledges that a floating point multiply accumulator (FMAC) is well understood by one skilled in the art to be a hardware module that is part of an electronic device such as a central processing unit. *See* Appeal Br. 3 (citing Spec. 11:10–15). Implementing an abstract idea on generic hardware or a generic processor is

not a practical application of the abstract idea. *See Alice*, 573 U.S. at 221; *see also Gottschalk v. Benson*, 409 U.S. 63 (implementing a mathematical principle on a general purpose computer is a patent ineligible abstract idea).

We are not persuaded by Appellant's arguments analogizing the subject matter of claim 8 with the facts before the Federal Circuit in *Enfish*. *See* Appeal Br. 3–5 (citing *Enfish*). We agree with the Examiner that *Gottschalk v. Benson* draws a more appropriate comparison to claim 8 than *Enfish*. *See* Ans. 3. In *Gottschalk v. Benson*, the Court focused on the claimed invention, which the Court characterized as a method for converting binary-coded decimal (BCD) numerals into pure binary numerals. *See* 409 U.S. at 64. The Court found that mathematical formula involved no substantial practical application except in connection with a digital computer. *See id.* at 72. Appellant does not direct us to evidence sufficient to demonstrate that the claimed invention provides an improvement in computer capabilities, like *Enfish* where the Federal Circuit found a self-referential table in a computer database improved the computer functionality itself. Appellant's arguments and supporting citations to Appellant's Specification do not sufficiently address the mathematical calculations recited in claim 8, as improving the computer functionality itself. *See* Appeal Br. 3–4. In particular, page 6, lines 7 through 23 of the Specification, cited by Appellant in support of its arguments, discloses the use of *multi-precision mantissa alignment comprising two parallel single-precision operations (operation circuits)* that may allow for decreased latency in floating point multiply-add operations as well as higher throughput, and may allow power and/or area optimization for FMUCs. *See* Spec. 6:7–23. And page 12, lines 1 through 17 of the Specification, cited by

Appellant in support of its arguments, discloses mantissa alignment/equalization, the use of two parallel single-precision operation circuits for exponent addition and mantissa multiplication, in addition to mathematical calculations recited in claim 8, but is silent regarding any reduction in latency resulting from the mathematical calculations recited in claim 8. Similar to the citations provided by Appellant, the Specification also discloses that multi-precision mantissa alignment may alleviate or reduce barriers to power reduction, efficiency, and flexibility. *See* Spec. 2:17–18. Likewise, the Specification discloses that using parallel single-precision operations can improve power usage, overhead, efficiency, and flexibility, compared to state of the art FMUCs lacking parallel single-precision operations. *See id.* at 2:20–21. Multi-precision mantissa alignment and parallel single-precision operations (operation circuits), however, are not recited in claim 8. For these reasons, we are not persuaded that the mathematical calculations recited in claim 8 improve the functionality of the computer itself, rather than features not claimed (e.g., mantissa alignment or parallel single-precision operations) that may provide improvements. Accordingly, we agree with the Examiner that the mathematical calculations of claim 8 can be performed without any specific processor configuration necessitated by the mathematical calculations, and creates no structure, logical or otherwise, beyond generic processor structure. *See* Ans. 4–5.

Because we determine claim 8 does not integrate the judicial exception into a practical application, and is instead directed to an abstract idea, we analyze the claims under step two of *Alice* to determine if there are additional elements that individually, and as an ordered combination, ensure

the claims amount to "significantly more" than the abstract idea—an inventive concept. *See Alice*, 573 U.S. at 217–18 (citing *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 77–79 (2012)). As stated in the Guidance, many of the considerations to determine whether the claims amount to "significantly more" under step two of the *Alice* framework are already considered as part of determining whether the judicial exception has been integrated into a practical application. *See* Guidance, 84 Fed. Reg. at 56. Therefore, at this point of our analysis, we determine if the claims include a specific element, or an ordered combination of elements, that is not well-understood, routine, conventional activity in the field, or simply appends well-understood, routine, conventional activities at a high level of generality. *See id.* "Whether something is well-understood, routine, and conventional to a skilled artisan at the time of the patent is a factual determination." *Berkheimer v. HP Inc.*, 881 F.3d 1360, 1369 (Fed. Cir. 2018).

In the case before us, claim 8 does not recite specific limitations, or an ordered combination of limitations, that are not well-understood, routine, and conventional. As discussed above, the sole additional element recited in claim 8 is "at a floating point multiply accumulator." And as briefly mentioned above, Appellant acknowledges that a floating point multiply accumulator (FMAC) is well understood by one skilled in the art to be a hardware module that is part of an electronic device such as a central processing unit. *See* Appeal Br. 3 (citing Spec. 11:10–15). Thus we conclude that the element of "at a floating point multiply accumulator" recited in claim 8 does not provide "significantly more" than the recited judicial exception.

For the foregoing reasons, we are not persuaded the Examiner erred in rejecting claims 8–13 under 35 U.S.C. § 101. Accordingly, we sustain the Examiner's rejection of claims 8–13 under 35 U.S.C. § 101 as directed to patent-ineligible subject matter.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Basis	Affirmed	Reversed
8–13	101	Eligibility	8–13	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED