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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DANIEL K. HILTGEN and RENE W. SCHMIDT

Appeal 2019-000077
Application 15/167,949
Technology Center 2100

Before JOHN A. JEFFERY, BRADLEY W. BAUMEISTER, and DENISE M. POTHIER, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's decision to reject claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b). We AFFIRM.

STATEMENT OF THE CASE

Appellant's invention (1) represents virtual primary disk data and a virtual machine's state data in a storage unit; (2) exposes the virtual primary disk data of the virtual machine to a virtual machine's guest to allow the

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as VMware, Inc., Palo Alto, California and VMware, Inc. Appeal Br. 3.

guest to access the virtual primary disk data; and (3) prevents the guest from accessing the virtual machine's state data. *See* Abstract. Claim 5 is illustrative:

> 5. An apparatus comprising:
>
> a communication interface; and
>
> a storage unit coupled to the communication interface and containing a partition that includes at least state data of a virtual machine;
>
> a virtualization system hosting a virtualization layer and including at least one virtual machine supported by the virtualization layer, the at least one virtual machine having a guest running therein;
>
> wherein the virtualization layer secures state data of a virtual machine by:
>
> intercepting a read access from the guest, the read access including a location in the partition to be accessed;
>
> modifying the location to be accessed;
>
> sending the modified request to the storage unit via the communication interface to prevent the read access when the read access is for accessing the state data of the virtual machine, wherein the state data comprises at least instruction and value data that are stored in RAM, cache and registers of the virtual machine.

RELATED APPEAL

This application is a continuation of Application 11/960,524 ("'524 application") where we affirmed the Examiner's rejection of then-pending claims 1–45 in part. *Ex parte Hiltgen*, Appeal No. 2013-010164

(PTAB Dec. 9, 2015) ("Bd. Dec."). In that appeal, the Examiner's reliance on the Worley reference (cited below) was at issue, as is the case here

THE REJECTIONS

The Examiner rejected claims 1, 5, and 7 under 35 U.S.C. § 103 as unpatentable over Neiger (US 2007/0156986 A1; published July 5, 2007), Van Dyke (US 6,321,314 B1; issued Nov. 20, 2001), and Worley, Jr. (US 2007/0106986 A1; published May 10, 2007). Final Act. 3–12.[2]

The Examiner rejected claims 2–4 under 35 U.S.C. § 103 as unpatentable over Neiger, Van Dyke, Worley, and Hummel (2008/0114916 A1; published May 15, 2008). Final Act. 13–16.

The Examiner rejected claims 6, 8, 9, and 15 under 35 U.S.C. § 103 as unpatentable over Neiger, Van Dyke, Worley, and Edwards (US 2009/0300605 A1; published Dec. 3, 2009). Final Act. 16–21.

The Examiner rejected claims 10, 11, 16, and 17 under 35 U.S.C. § 103 as unpatentable over Neiger, Van Dyke, Worley, Edwards, and Fitzgerald (US 8,234,640 B1; issued July 31, 2012). Final Act. 22–26.

The Examiner rejected claims 12–14 and 18–20 under 35 U.S.C. § 103 as unpatentable over Neiger, Van Dyke, Worley, and Fitzgerald. Final Act. 26–30.

[2] Throughout this opinion, we refer to (1) the Final Rejection mailed June 15, 2017 ("Final Act."); (2) the Appeal Brief filed March 15, 2018 ("Appeal Br."); (3) the Examiner's Answer mailed August 7, 2018 ("Ans."); and (4) the Reply Brief filed October 2, 2018 ("Reply Br.").

THE REJECTION OVER NEIGER, VAN DYKE, AND WORLEY

Regarding representative independent claim 5, the Examiner finds that Neiger discloses the recited communication interface and virtualization system including a virtual machine supported by a virtualization layer that secures a virtual machine's state data by intercepting a read access including a location in a partition to be accessed. Final Act. 6–8. Although the Examiner acknowledges that Neiger does not modify this location or send the modified request to a storage unit to prevent the read access as claimed, the Examiner cites Van Dyke for teaching this feature. *Id.* 8–9. The Examiner also cites Worley for teaching a storage unit containing a partition that includes the virtual machine's state data, where the state data comprises at least instruction and value data stored in RAM, cache, and registers of the virtual machine. *Id.* 10–12. In light of these collective teachings, the Examiner concludes that the claim would have been obvious. Final Act. 6–12.

Appellant argues that the cited prior art does not teach or suggest preventing the read access when accessing the virtual machine's state data comprising at least instruction data and value data stored in RAM, cache, and registers of the virtual machine as claimed. Appeal Br. 7–11; Reply Br. 2–4. According to Appellant, the Examiner's reliance on Worley in this regard is misplaced, for not only are the critical data structures in Worley's paragraph 84 said to be non-analogous to the recited virtual machine state data, but the operation of Worley's virtual machine monitor (VMM) and Itanium processor also do not describe the recited state data. Appeal Br. 7; Reply Br. 3. Although Appellant acknowledges that various architectural features associated with Worley's Itanium processor, including privileged

instructions, translation look-aside register buffers (TLBs),[3] and privileged registers, may have some bearing on the physical processor's state, Worley is nevertheless said to be silent about the state of the virtual processor or virtual machine. Appeal Br. 7–9. Appellant adds that Worley's memory compartments in paragraph 84 are not analogous to the recited partition. Reply Br. 3–4.

ISSUE

Under § 103, has the Examiner erred in rejecting claim 5 by finding that Neiger, Van Dyke, and Worley collectively would have taught or suggested (1) a storage unit containing a partition including at least a virtual machine's state data, and (2) a virtualization layer preventing the read access when that access is for accessing the virtual machine's state data comprising "at least instruction and value data stored in RAM, cache[,] and registers of the virtual machine" (the "virtual machine state data limitation")?

ANALYSIS

We begin by noting that the Examiner's reliance on the Neiger and Van Dyke references is undisputed, as is the cited references' combinability. Rather, as noted above, this dispute turns solely on the Examiner's reliance on Worley for teaching the recited partition and virtual machine state data limitations. Therefore, we confine our discussion to Worley.

[3] Although Appellant labels these buffers as "translation look aside buffers," we nonetheless refer to them using Worley's nomenclature in paragraph 51, namely "translation look-aside register buffers."

As noted previously, the Examiner's reliance on Worley was at issue in the related appeal, and while claim 5 here differs from the claims that were at issue in the related appeal, our findings and conclusions regarding Worley are nonetheless applicable here and are, in fact, the law of this case. *See* Manual of Patent Examining Procedure (MPEP) § 706.07(h)(XI)(A) (9th ed. Rev. 08.2017, Jan. 2018) (noting that the Board's decision becomes the "law of the case" in that it is controlling on the application under appeal *and later related applications*).

In our earlier decision, we affirmed the Examiner's anticipation rejection of independent claim 39 over Worley. That claim recited, in its entirety (and with our emphasis), "[a] non-transitory computer-readable storage medium storing a computer program product comprising [] virtualization code executable to intercept a read access from the guest and prevent the read access when the read access is for *accessing the state data of the virtual machine*, wherein the state data comprises *execution state data of the virtual machine*."

Our emphasis underscores a key aspect of this claim, namely that the virtualization code can intercept and prevent a read access for accessing a virtual machine's state data, notably the virtual machine's *execution state data*. In finding that Worley anticipated these limitations, we noted that by executing Worley's VMM on the hardware system in Figure 3, *the VMM's state* will be reflected in the system's variables, buffers, and registers—a system whose state is controlled by privileged instructions. Bd. Dec. 7–8. We added that the claim read on a hypothetical scenario where the hardware moves the virtual machine's state data in and out of the registers, TLBs, and caches. *Id.* 8.

These findings are applicable here and, notably, were made in light of the Specification's description of state data of a virtual machine in paragraph 1072 of the originally-filed parent '524 application, namely that this data indicates a virtual machine's execution state at a particular time whether suspended or not. *See* Spec. ¶ 72.[4] Our findings regarding Worley were also made in light of the Specification's example of this state data that indicates current data in all or part of a virtual machine's memory (e.g., instruction and/or value data in the virtual machine's RAM, cache, registers, etc.). *See id.; see also* Bd. Dec. 7–8.

Our findings also reasonably comport with those of the Examiner. Notably, the Examiner finds that Worley's privileged instructions, which are used to fill entries in the TLB, are protected by the VMM, and that this VMM-based functionality effectively controls (1) TLB entries; (2) status registers; and (3) other state controlling resources, thus rendering these elements analogous to the recited state data. Ans. 8–9 (citing Worley ¶¶ 14, 58). The Examiner adds that by controlling access to the instruction and data TLBs, the state data includes instructions and value data because privileged instructions control access to not only data *in* the TLBs, but also data *addressed by* the TLBs. Ans. 9 (citing Worley ¶¶ 58, 53).

Despite Appellant's arguments to the contrary, Appellant does not persuasively rebut these findings, particularly given the scope and breadth of the claim. That we found Worley disclosed preventing a read access when

[4] Paragraph 1072 of the parent '524 application's originally-filed Specification (and paragraph 77 of the corresponding published application US 2008/0155208 A1) is equivalent to paragraph 72 of the present application's Specification. For clarity, we refer to paragraph 72 unless otherwise indicated.

that access is for accessing *execution state data of a virtual machine* only bolsters the Examiner's findings in this regard. *See* Bd. Dec. 7–8. Nor does Appellant persuasively rebut the Examiner's finding that Worley's TLB is a RAM-based cache, and that Worley's VMM accesses and executes (1) privileged instructions and registers stored in instruction cache, and (2) value data stored in data caches in view of the Intel Itanium Architecture Software Developer's Manual. *See* Ans. 10–11. To the extent that Appellant contends that this functionality pertains to only the physical state of the Itanium processor, and not that of a virtual machine including the recited state data (*see* Appeal Br. 8–9), we disagree, for this contention ignores our earlier decision where we found, among other things, that executing Worley's VMM on the hardware system in Figure 3 reflects *the VMM's state* in the system's variables, buffers, and registers. Bd. Dec. 7–8. Appellant's arguments in this regard are, therefore, unavailing and not commensurate with the scope of the claim.

Nor does Appellant persuasively rebut the Examiner's reliance on Worley's paragraph 44 for at least suggesting the recited storage unit contains a partition including at least state data of a virtual machine. *See* Final Act. 10. As the Examiner indicates, Worley's operating system creates an illusion of relatively vast virtual-memory address spaces by storing data on mass storage devices 508, where the data are addressed via a virtual-memory address space. *Id.* (citing Worley ¶ 44). Appellant does not squarely address—let alone persuasively rebut—these particular findings to show error in the Examiner's rejection in this regard.

Notably, Appellant's arguments regarding the alleged shortcomings of Worley's memory compartments in paragraph 84 that store critical data

structures in connection with the recited partition and state data (Reply Br. 3–4) are not germane to the Examiner's reliance on the above-noted functionality in Worley's paragraph 44 in this regard on page 10 the Final Office Action. We reach this conclusion even if we were to accept Appellant's argument on pages 3 and 4 of the Reply Brief that the Examiner erred by relying on Worley's memory compartments and critical data in paragraph 84 for teaching the recited partition and state data in the Answer. Despite these contentions, Appellant still does not squarely address—let alone persuasively rebut—the Examiner's *alternative* findings in this regard articulated on page 10 of the Final Office Action from which this appeal was taken. Accordingly, the weight of the evidence on this record favors the Examiner.

Therefore, we are not persuaded that the Examiner erred in rejecting claim 5, and claims 1 and 7 not argued separately with particularity.

THE REJECTION OVER NEIGER, VAN DYKE, WORLEY, AND EDWARDS

We also sustain the Examiner's rejection of claim 6 reciting that the partition includes a virtual disk for the virtual machine and the virtualization layer exposes the virtual disk to the virtual machine's guest. Although Appellant contends that Edwards lacks a partition that includes *both* state data *and* a virtual disk for a virtual machine (Appeal Br. 11–12; Reply Br. 4–5), the Examiner's rejection is not based on Edwards alone, but rather Worley and Edwards collectively for at least suggesting this limitation. That is, as noted previously, the Examiner cites (1) Worley for teaching a storage unit containing a partition including at least a virtual machine's state data,

and (2) Edwards for teaching that virtual disks for virtual machines are known in the art, and that providing a virtual disk in connection with Worley's partition would have been obvious. *See* Final Act. 16–17; Ans. 13–14 (noting that Worley shows a partition for state data, and that modifying this partition in light of Edwards would have been obvious).

Such an enhancement uses prior art elements predictably according to their established functions—an obvious improvement. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (2007). Appellant's arguments regarding Edwards' individual shortcomings in this regard (App. Br. 11–12; Reply Br. 4–5) do not show nonobviousness where, as here, the rejection is based on the cited references' collective teachings. *See In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

Therefore, we are not persuaded that the Examiner erred in rejecting claim 6, and claims 8, 9, and 15 not argued separately with particularity.

THE OTHER OBVIOUSNESS REJECTIONS

We also sustain the Examiner's obviousness rejections of claims 2–4, 10–14, and 16–20. Final Act. 11–26. Because these rejections are not argued separately with particularity, we are not persuaded of error in these rejections for the reasons previously discussed.

CONCLUSION

In Summary:

Claims Rejected	Basis	Affirmed	Reversed
1–20	§ 103 Neiger, Van Dyke, Worley	1, 5, 7	
	§ 103 Neiger, Van Dyke, Worley, Hummel	2–4	
	§ 103 Neiger, Van Dyke, Worley, Edwards	6, 8, 9, 15	
	§ 103 Neiger, Van Dyke, Worley, Edwards, Fitzgerald	10, 11, 16, 17	
	§ 103 Neiger, Van Dyke, Worley, Fitzgerald	12–14, 18–20	
Overall Outcome		1–20	

AFFIRMED