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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte GOERAN SCHUBERT, ANDREAS PSCHORR, DIEGO ANTONGIROLAMI, and ULRICH BLEY

Appeal 2018-009041
Application 14/759,051
Technology Center 2800

Before BRADLEY R. GARRIS, KAREN M. HASTINGS, and JAMES C. HOUSEL, *Administrative Patent Judges*.

HOUSEL, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to finally reject claims 17–27 and 29–34[2] under 35 U.S.C. § 102(a)(1) as anticipated by Lalithambika (US 8,411,468 B2, iss. Apr. 2, 2013). We have jurisdiction under 35 U.S.C. § 6(b).

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Conti Temic Microelectronic GmbH, which is a daughter of Continental AG. Br. 1.

[2] The Examiner states that pending claim 35 is allowed in the Advisory Action dated July 27, 2017, but indicates, in error, that this claim is rejected in the Notice of Panel Decision from Pre-Appeal Brief Review dated January 8, 2018.

We AFFIRM.[3]

STATEMENT OF THE CASE

The invention relates to methods for switching an electronic component on or off under the control of a pulse-width-modulation ("PWM") signal. Spec. 1:2–3. Appellant discloses that inductive electrical loads such as DC motors are often controlled by PWM in order to adjust current and/or voltage for the respective electrical load. *Id*. at 1:4–6. For this purpose, the load is often coupled in a resonant full- or half-bridge circuit to metal-oxide semiconductor field-effect transistors (MOSFETs) or insulated-gate bipolar transistors (IGBTs) which are switched on and off under the control of the PWM signal to adjust the current and/or voltage of the load. *Id*. at 1:6–11. However, when such components are switched on and off, undesired parasitic oscillations of the current and voltage can occur, which can negatively affect the electromagnetic compatibility of the circuit and cause switching losses. *Id*. at 1:11–14. According to Appellant, the inventive method addresses this problem and leads to a reduction in parasitic oscillations. *Id*. at 1:24–26.

Claim 17, reproduced below from the Claims Appendix to the Appeal Brief, is illustrative of the subject matter on appeal.

> 17. A method of switching an electronic component on or off under the control of a pulse-width-modulation signal, the electronic component being configured to output an output signal controlled by way of a control signal, the method comprising:

[3] Our Decision refers to the Specification ("Spec.") filed July 2, 2015, the Examiner's Final Office Action ("Final Act.") dated May 5, 2017, Appellant's Appeal Brief ("Br.") filed Mar. 8, 2018, and the Examiner's Answer ("Ans.") dated July 10, 2018.

> initiating the switching on or off within a pulse-width-modulation clock period at a level-change instant by a change in the pulse-width-modulation signal;
>
> calculating at least one amplitude magnitude of an oscillation of the output signal during each clock period of the pulse-width-modulation signal;
>
> predefining at least one first control value and one second control value of the control signal;
>
> adjusting the control signal to the first control value within each pulse-width-modulation clock period between the level-change instant and a first switchover instant and adjusting the control signal to the second control value between the first switchover instant and a second switchover instant and adjusting the control signal to a third control value from the second switchover instant until a gate voltage end value of a gate voltage is reached at a control connection of the electronic component; and
>
> determining each of the first and second switchover instants of a pulse-width-modulation clock period on a basis of an amplitude magnitude associated with the pulse-width-modulation clock period and calculated during a preceding pulse-width-modulation clock period, to thereby limit oscillation amplitudes of an oscillation of the output signal.

Remaining independent claim 34 recites a similar method to claim 17 except that the method requires that the electronic component is repeatedly switched on and off.

ANALYSIS

After review of the Examiner's and Appellant's opposing positions and the appeal record before us, we determine that Appellant's arguments are insufficient to identify reversible error in the Examiner's anticipation rejection. *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011). Accordingly, we affirm the stated anticipation rejection for substantially the fact findings

and the reasons set forth by the Examiner in the Examiner's Answer and the Final Office Action. We offer the following for emphasis only.

Appellant presents substantially the same arguments against the rejection of both claims 17 and 34. *Compare* Br. 7–9 *and* Br. 9–11. In accordance with 37 C.F.R. § 41.37(c)(1)(iv), the claims subject to the anticipation rejection stand or fall with claim 17, which we select as representative in our opinion below.

The Examiner finds that Lalithambika teaches a method of switching an electronic component on or off under the control of a PWM signal as recited in claim 17, wherein the component is configured to output a signal controlled by a control signal. Final Act. 3–4 (citing Lalithambika Figs. 15 and 20, Spec. 12:3–4, 12–18, 58–67, 13:1–6).

Appellant argues that Lalithambika's Figure 15 fails to show a calculation of a magnitude of an oscillation. Br. 7. Appellant asserts that Lalithambika instead shows a peak detector, which measures a voltage across capacitor C_{peak}, and an Error Amplifier 1204, which compares a reference voltage V_{REF} to the voltage across capacitor C_{peak}. *Id*. Appellant further asserts that a value is obtained and, based on the value relative to the reference value, a signal (0 or 1) is sent to the PWM 610. *Id*. Appellant contends that Lalithambika uses this value not to determine switchover instants of a PWM clock period, but to apply a base current. *Id*. at 8. Appellant also asserts that, though having a cycle to cycle memory that determines a base drive, Lalithambika does not calculate amplitude magnitude of an oscillation of the output during each cycle. *Id*.

Appellant further argues that the Examiner's explanation that Lalithambika uses the amplitude magnitude of an oscillation signal to

determine switchover instants of a PWM clock period is an oversimplification of Appellant's argument and claimed invention. Br. 9. Appellant urges that Lalithambika's leaky peak detector, as shown in Figure 15, feeds its output signal to an op-amp 1204, which essentially is a gate that drives the PWM 610 does not anticipate claim 17 which requires calculation of the amplitude magnitude and limits the next following oscillation amplitude on the basis of this amplitude magnitude. *Id*.

The Examiner responds that Lalithambika teaches calculating at least one amplitude magnitude of an oscillation of the output signal during each clock period of the PWM signal via the leaky peak detector of Figure 15 because this detector calculates the peak amplitude of the output of the sensing element 212. Ans. 2. The Examiner further responds that Lalithambika teaches using the amplitude magnitude of an oscillation signal of the output signal, again via the leaky peak detector of Figure 15, to determine switchover instants of a PWM clock period. *Id*. at 3, citing to Lalithambika, Fig. 20, 19:23–25. In addition, the Examiner finds that Lalithambika teaches that peak detector maintains a level of the base drive so that in a subsequent cycle, the base drive is applied soon enough in the on period to sustain heavy loads later, which the Examiner determines is a calculation of the amplitude magnitude during each clock period of the PWM signal. *Id*., citing Lalithambika 12:16–18, 12:64–67; 14:19. Finally, the Examiner finds that Lalithambika provides a wider range of control and reduces problems associated with inductive loads. *Id*.

During examination, the Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). On appeal, the initial burden is on Appellant to

identify reversible error. *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011) ("[E]ven assuming that the examiner had failed to make a prima facie case, the Board would not have erred in framing the issue as one of 'reversible error.'"); *cf Shinseki v. Sanders*, 129 S.Ct. 1696, 1706 (2009) (citations omitted) ("Lower court cases make clear that courts have correlated review of ordinary administrative proceedings to appellate review of civil cases in this respect. . . . [T]he party seeking reversal normally must explain why the erroneous ruling caused harm.") As a result, the burden is on Appellant to come forward with persuasive arguments and/or evidence to rebut the prima facie case of anticipation. *In re Dillon*, 919 F.2d 688, 692 (Fed. Cir. 1990).

Here, Appellant merely repeats the same arguments raised to the Examiner during prosecution without explaining or elaborating why the Examiner's response to those arguments in the Answer is incorrect or otherwise in error. For example, Appellant fails to establish reversible error in the Examiner's finding that Lalithambika's leaky peak detector does not calculate the amplitude magnitude of each oscillation by determining the peak amplitude of the output of the sensing element. Appellant also fails to explain why the Examiner's finding that Lalithambika teaches using the amplitude magnitude of an oscillation signal of the output signal, via the leaky peak detector, to determine switchover instants of a PWM clock period as shown in Figure 20 is erroneous. Under these circumstances, Appellant has not carried their burden to identify reversible error in the Examiner's finding of anticipation.

Accordingly, we sustain the Examiner's anticipation rejection of claims 17–27 and 29–34.

DECISION

Upon consideration of the record, and for the reasons given above and in the Final Office Action and the Examiner's Answer, the decision of the Examiner rejecting claims 17–27 and 29–34 under 35 U.S.C. § 102(a)(1) as anticipated by Lalithambika is *affirmed*.

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

CONCLUSION

In summary:

Claims Rejected	**Basis**	**Affirmed**	**Reversed**
17–27, 29–34	§ 102(a)(1); Lalithambika	17–27, 29–34	

AFFIRMED