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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte YONG-HO JANG, BINN KIM, HAE-YEOL KIM, and BU-YEOL LEE

Appeal 2018-008844[1]
Application 13/727,251
Technology Center 2600

Before HUNG H. BUI, ADAM J. PYONIN, and MICHAEL M. BARRY, *Administrative Patent Judges*.

PYONIN, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

[1] The real party in interest is listed as LG Display Co., Ltd. App. Br. 2.

STATEMENT OF THE CASE

Introduction

The Application relates to "an image display device including . . . a gate driver capable of improving reliability without using a complicated waveform for driving pixels by simplifying the structure of a shift register." Spec. ¶ 2. Claims 1–9, 12, and 13 are pending; of these, claims 1 and 5 are independent. App. Br. 32–35. Claim 1 is reproduced below for reference (emphasis added):

> 1. A gate driver comprising: a plurality of driving units connected to respective rows of pixels of a display area, each of the driving units including:
>
> a first sub driving unit having an output terminal connected to a first sub gate line of a respective row of pixels, the output terminal of the first sub driving unit supplies a first sub output to gate terminals of first switching transistors in each pixel of the respective row of pixels, and
>
> *a second sub driving unit having an output terminal connected to a second sub gate line of the respective row of pixels, the output terminal of the second sub driving unit supplies a second sub output to gate terminals of second switching transistors in each pixel of the respective row of pixels, source and drain terminals of the second switching transistors being connected to corresponding source and drain terminals of the first switching transistors in each of the pixels,*
>
> *wherein a first data signal to be displayed is applied to a pixel of the row when the first output of the first sub driving unit is present and a second data signal to be displayed is applied to the pixel when the second output of the second sub driving unit is present,*
>
> wherein a time when the first switching transistor is turned on by a first pulse of the first sub output in a frame does not overlap a time when the second switching transistor is turned on by the second sub output in the frame,

> wherein the output of the first sub driving unit is present every frame, and the output of the second sub driving unit is present every N frames (where N is a number of second sub gate lines),
>
> wherein each of the first and second sub driving units includes an input unit that receives a start signal and a reset signal that control driving of the first and second sub driving units, and
>
> wherein the start signal to the input unit of the first sub driving unit is the output of the first sub-driving unit at a previous stage except for the input unit of the first sub driving unit in a first stage, the same output of the first sub-driving unit is also applied to the gate terminal of the first transistor to turn on the first transistor.

References and Rejections

Claims 1–9, 12, and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jang (US 2006/0145991 A1; July 6, 2006), Kitazawa (US 2008/0036706 A1; Feb. 14, 2008), and Applicant Admitted Prior Art (AAPA). Final Act. 3.

ANALYSIS

We have reviewed the Examiner's rejection in light of Appellants' arguments. Arguments Appellants could have made but chose not to make are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(iv).

Appellants argue the Examiner's rejection is in error:

> one having ordinary skill in the relevant field would not be motivated in any way to modify the pixel precharge transistor (M3) and the write transistor (M2) of Kitazawa in such a way as "to send two different data signals by using two parallel transistors instead [of] pulsing a single transistor twice to send two different data signals which would offer a substitute method to achieve the predictable result of transmitting two different data signals to the same pixel," as alleged by the Examiner. *See*

> Office Action at pp. 9–10. . . . *[N]one of the references in any combination teach or suggest applying two different data signals to be displayed by two different transistors*. Only Kitazawa teaches two different transistors, but only one of those transistors (i.e., the write transistor (M2)) is capable of applying a data signal to be displayed, while the other transistor is only operable to precharge the coupling capacitor (Cc). In contrast, data that is "written into the pixel" is supplied from the write transistor (M2) and is held in the first holding capacitor (ch l). *See* Kitazawa at ¶ [151].

App. Br. 27–28 (emphasis modified).

We agree. Claim 1 recites first and second "sub driving unit[s]," each connected to a respective switching transistor of parallel transistors in the same "pixel of the respective row of pixels." The Examiner finds the claimed device "can be done by using the gate driving circuit of Jang combining with the parallel transistor pixel circuit of Kitazawa" (Final Act. 16; Jang ¶¶ 47–49), because the "use of a single switch to transmit [a] signal serially or use of two parallel switches to transmit [the] signal involves only the most basic electrical knowledge possessed by anyone of ordinary skilled in the art" (Ans. 9; *see also* Final Act. 23; Kitazawa Fig. 8 (depicting first and second transistors M2 and M3)). We find such analysis to be insufficient to support the determination of obviousness.

As noted by Appellants, Jang's sub driving units are each connected to a different row of pixels, and both Jang and Kitazawa use only one switching transistor for supplying a data signal to be displayed. *See* App. Br. 27; Jang Fig. 7; ¶ 42; Kitazawa ¶ 131. That is, the references do not disclose or teach using two switching transistors in place of one, and the Examiner provides no reason to modify Jang to send data signals to the same pixel based on signals from two different sets of sub driving units and

switching transistors. Rather, the Examiner merely states the combination "achieve[s] the predictable result" (Final Act. 10) and "is obvious to try" (Ans. 9), without explaining *why* one of ordinary skill would combine the references as claimed. Thus, we agree with Appellants the "Examiner . . . impermissibly relies on hindsight reasoning, using the teachings that can only be gleaned from Appellant's own disclosure, in combining the cited references." App. Br. 28; *see KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 421 (2007) ("A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."); *see also In re Chaganti*, 554 F. App'x 917, 922 (Fed. Cir. 2014) ("It is not enough to say that there would have been a reason to combine two references because to do so would 'have been obvious to one of ordinary skill.' Such circular reasoning is not sufficient—more is needed to sustain an obviousness rejection.").

Accordingly, we do not sustain the Examiner's obviousness rejection of independent claim 1, of independent claim 5 which recites limitations commensurate in scope (*see* Final Act. 13), or the claims dependent thereon.

DECISION

The Examiner's decision rejecting claims 1–9, 12, and 13 is reversed.

REVERSED