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Marc P. Schuyler
P.O. Box 2535
Saratoga, CA 95070

EXAMINER	
AHMED, ZUBAIR	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ANDREY V. KUZMIN, ALAN CHEN, and ROBERT LERCARI

Appeal 2018-008814
Application 14/848,273
Technology Center 2100

Before MARC S. HOFF, IRVIN E. BRANCH, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

SZPONDOWSKI, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1, 5, 8, 9, 11–13, 17, 20, and 22–44, constituting all claims pending in the application. Claims 2–4, 6, 7, 10, 14–16, 18, 19, and 21 have been cancelled. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Radian Memory Systems, Inc. Appeal Br. 1.

STATEMENT OF THE CASE

Appellant's invention generally relates to "data placement and migration techniques that facilitate more efficient integration and utilization of nonvolatile memory, especially flash-based storage, in heterogeneous storage systems." Spec. ¶ 2. Claim 1, reproduced below, is representative of the claimed subject matter:

> 1. A memory controller integrated circuit to control nonvolatile memory, comprising:
>
> an interface to receive commands from a host;
>
> logic to update metadata values for respective logical addresses corresponding to data stored in the nonvolatile memory in response to data access operations commanded by the host, to identify a subset of the one or more of the metadata values which meet at least one criterion and, in response to identification of the one or more metadata values meet the at least one criterion, to transmit to the host a notification; and
>
> logic to maintain wear information associated with independently erasable units of physical memory locations in the nonvolatile memory, and to identify at least one of the independently erasable units dependent on the respective wear information as a candidate relocation target destination in which to relocate data within the nonvolatile memory which corresponds to a specific logical address to a different physical storage location, the data corresponding to the specific logical address selected dependent on the subset;
>
> wherein each metadata value represents at least one of prior read of data associated with a corresponding one of the logical addresses, frequency of read of the data associated with the corresponding one of the logical addresses, age since last write of the data associated with the corresponding one of the logical addresses, or frequency of write of the data associated with the corresponding one of the logical addresses;

> wherein the memory controller integrated circuit is to receive a command from the host to move the data corresponding to the specific logical address in response to the notification to the host; and
>
> wherein the memory controller integrated circuit comprises logic to execute the move of the data corresponding to the specific logical address to the candidate relocation target destination in response to the command to move.

REJECTIONS

Claims 1, 5, 8, 9, 12, 13, 17, 20, 22–26, 29–33, and 36–38 stand rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over the combination of Rub et al. (US 2013/0007343 A1; published Jan. 3, 2013) ("Rub"), Merry et al. (US 2007/0260811 A1; published Nov. 8, 2007) ("Merry"), and Wakrat et al. (US 2012/0191664 A1; published July 26, 2012) ("Wakrat").

Claims 11 and 39–44 stand rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over the combination of Rub, Merry, Wakrat, and Cohen et al. (US 2014/0208004 A1; published July 24, 2014) ("Cohen").

Claims 27 and 34 stand rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over the combination of Rub, Merry, Wakrat, and Eleftheriou et al. (US 2012/0131381 A1; published May 24, 2012) ("Eleftheriou").

Claims 28 and 35 stand rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over the combination of Rub, Merry, Wakrat, and Kunimatsu et al. (US 2009/0083478 A1; published Mar. 26, 2009) ("Kunimatsu").

ANALYSIS

Appellant argues, *inter alia*, that the combination of Rub, Merry, and Wakrat does not teach or suggest "wherein the memory controller integrated circuit is to receive a command from the host to move the data corresponding to the specific logical address in response to the notification to the host" and "wherein the memory controller integrated circuit comprises logic to execute the move of the data corresponding to the specific logical address to the candidate relocation target destination in response to the command move," as recited in independent claim 1 and commensurately recited in independent claims 13 and 38. Appeal Br. 15–20, 26–27; Reply Br. 2–4.

The Examiner relies on Merry to teach or suggest the disputed limitations. Final Act. 8–10; Ans. 21–26. Specifically, the Examiner finds Merry teaches two types of wear leveling operations that the memory controller performs at the behest of the host system. Ans. 22–23. First, the Examiner finds Merry "remaps LBAs from more worn physical data blocks to less worn physical data blocks . . . based on data access frequency which clearly requires physical moving of data for more worn physical data blocks to less worn physical data blocks." Ans. 23 (citing Merry ¶ 50). Second, the Examiner finds Merry "redirects new writes to determined physical data blocks based on wear information of the physical data blocks and the frequency of write operations." Ans. 23 (citing Merry ¶ 52); *see also* Ans. 8 (Merry's "storage manager program 615 (FIG. 6), which runs on host 110 (FIG. 6) directs or commands wear management operations to be carried out by the memory controller 114 (FIG. 1) using device driver 113 (FIG. 1)).

The Examiner finds that "both types of wear leveling operations . . . include[] moving of physical data from one location to another location as required by the claims." Ans. 23.

Appellant argues that Merry does not teach the disputed limitations. Appeal Br. 15–20, 26–27; Reply Br. 2–4. Appellant argues Merry does not teach that the host sends a command to the memory controller to move data or that the memory controller comprises logic to execute a move of data in response to a command to move, as claimed. Appeal Br. 18–20. Rather, Appellant contends Merry teaches (1) that Merry's "memory controller can perform conventional wear leveling (i.e., transparent to a host)" and (2) that the host "diverts new writes of data to a different storage drive, i.e., to a different memory controller (or perhaps the worn drive for very cold data – *see* ¶¶ 51–53)." Appeal Br. 19–20.

We are persuaded by Appellant's arguments. Merry is generally directed to maintaining usage statistics reflective of the wear state of a non-volatile solid-state storage system, and using that information for various purposes. Merry Abstract. Merry describes the use of wear leveling to "prevent failures due to repeated program/erase cycles in high-volume locations." Merry ¶ 41. "Wear leveling is generally used to map the same logical data to different physical locations," for example, "changing the logical-to-physical address mapping of one or more data blocks 402 so as to direct future high-volume re-writes to data blocks 402 that have historically been used less often." Merry ¶ 42. Merry discloses that "the controller 114 performs wear leveling on the corresponding data block 402 by remapping corresponding logical addresses to different physical locations in other data blocks 402." Merry ¶ 50. The Examiner has not provided sufficient support

that this wear leveling "clearly requires" physical *moving* of data, or that it is at the "behest" of the host.[2] *See* Ans. 23, 26. Merry also discloses that storage manager program 615 in host system 110 may perform wear leveling, for example "the storage manager 615 may choose to direct data storage to the second subsystem so as to reduce wear on the first storage system 112." Merry ¶¶ 51–52. Here, again, the Examiner has not provided sufficient support that this wear leveling "includes moving of physical data from one location to another location" or is executed by the memory controller at the behest of the host. *See* Ans. 23–25. In other words, in both types of wear leveling described in Merry, the data is *redirected* rather than *moved*. The Examiner, therefore, has not sufficiently explained how the two types of wear leveling operations described in Merry teach or suggest that the memory controller "is to receive a command from the host to move the data corresponding to the specific logical address in response to the notification to the host" or that the memory controller "comprises logic to execute the move of the data corresponding to the specific logical address to the candidate relocation target destination in response to the command to move."

Appellant presents additional arguments. However, because the identified issue is dispositive of the appeal with regard to the rejections under 35 U.S.C. § 103(a), we do not reach these additional arguments. Accordingly, we are persuaded on this record that the Examiner erred in

[2] Moving data is only mentioned in paragraph 45 of Merry, which is not relied upon or discussed by the Examiner. We agree with Appellant that it appears the host is not involved in these move operations. *See* Appeal Br. 18.

rejecting independent claims 1, 13, and 38, for the reasons discussed above, and dependent claims 2, 5, 8, 9, 11, 12, 17, 20, 22–37, and 39–44, for the same reasons.

CONCLUSION

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1, 5, 8, 9, 12, 13, 17, 20, 22–26, 29–33, 36–38	103(a)	Rub, Merry, Wakrat		1, 5, 8, 9, 12, 13, 17, 20, 22–26, 29–33, 36–38
11, 39–44		Rub, Merry, Wakrat, Cohen		11, 39–44
27, 34		Rub, Merry, Wakrat, , Eleftheriou		27, 34
28, 35		Rub, Merry, Wakrat, Kunimatsu		28, 35
Overall Outcome				1, 5, 8, 9, 11–13, 17, 20, and 22–44

REVERSED