



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/336,554	10/27/2016	Ian Shaeffer	RA992.C1C1.US	1628
38489	7590	11/26/2019	EXAMINER	
SILICON EDGE LAW GROUP, LLP 7901 Stoneridge Drive Suite 528 PLEASANTON, CA 94588			OJHA, AJAY	
			ART UNIT	PAPER NUMBER
			2824	
			NOTIFICATION DATE	DELIVERY MODE
			11/26/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
art@siliconedgelaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte IAN SHAEFFER

Appeal 2018-008415
Application 15/336,554
Technology Center 2800

Before GRACE KARAFFA OBERMANN, DONNA M. PRAISS, and
SHELDON M. MCGEE, *Administrative Patent Judges*.

MCGEE, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant¹ appeals from the
Examiner's decision to reject claims 2–4 and 6–21. We have jurisdiction.
35 U.S.C. § 6(b).

We affirm.

¹ We use the word Appellant to refer to “applicant” as defined in 37 C.F.R.
§ 1.42(a). Appellant identifies the real party in interest as Rambus Inc. Br. 1.

SUBJECT MATTER

The subject matter on appeal “relates generally to high-speed electronic signaling in support of memory access.” Spec. ¶ 1. Claim 2 is illustrative of the claimed subject matter, and is reproduced below with key limitations italicized:

2. A width-configurable memory module to respond to commands from a memory controller, *the commands including a chip-select signal* and directed to a rank of memory devices, wherein a rank refers to a number of the memory devices used for each of the commands, the module comprising:

module data-group ports to communicate first data and second data to the memory controller;

a first rank group of first memory devices to store the first data, the first rank group having a first subset of the number of the memory devices used for each of the commands;

a second rank group of second memory devices to store the second data, the second rank group having a second subset of the number of the memory devices used for each of the commands;

a register to store at least one of a first value indicative of a first module width and a second value indicative of a second module width greater than the first module width;

a command router coupled to the register, the first memory devices, and the second memory devices, the router:

to alternatively access, *responsive to the chip-select signal*, only one of the first and second rank groups, each access to communicate either the first data from the first memory devices or the second data from the second memory devices over a first subset of the module data-group ports responsive to the first value indicative of the first module width; and

to simultaneously access both the first and second rank groups, each access to communicate the first data

from the first memory devices over the first subset of the module data-group ports and the second data from the second memory over a second subset of the module data-group ports responsive to the second value indicative of the second module width.

Br. 12 (Claims Appendix) (emphases added).

REFERENCES

The Examiner relies on the following prior art:

Name	Reference	Date
Yoo	US 2002/0129215 A1	Sept. 12, 2002
Ware	US 2005/0166026 A1	July 28, 2005

REJECTIONS²

The following rejections are before us on appeal:

- I. Claims 2–4, 6–17, and 21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ware; and
- II. Claims 18–20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the combined disclosures of Ware and Yoo.

² The Examiner’s Answer states that “[e]very ground of rejection set forth in the Office Action dated 08/28/2017 from which the appeal is taken is being maintained.” Ans. 3. The Answer then identifies the rejection of claims 2–4, 6–17, and 21 as unpatentable over Ware, but does not specifically list the rejection of claims 18–20 over Ware and Yoo as being maintained or withdrawn. *Id.* Therefore, in view of the Examiner’s general statement that the rejections set forth in the August 28, 2017 Final Action are being maintained “except for the grounds” identified as “withdrawn,” we treat the rejection of claims 18–20 as maintained and properly before us.

OPINION

Rejection I

The Examiner’s findings regarding how the embodiments of Ware disclose the limitations of the claims subject to this rejection appear at pages 3–14 of the Final Office Action dated August 28, 2017. Specifically, and relevant to the appeal of this rejection, the Examiner finds Ware discloses “commands including a chip-select signal” and that Ware’s command router, responsive to such chip-select signals, performs the functions set forth in independent claims 2 and 12. Final Act. 3–6, 11 (citing Ware ¶ 77, Figs. 5B, 6A). The Examiner acknowledges that Ware does not disclose all claim limitations recited in independent claims 2 and 12 in one embodiment, but determines the skilled artisan would have found it obvious “to combine teachings from various embodiments to provide memory modules and methods with flexibility to scale bandwidth.” *Id.* at 7, 12.

Regarding claim 2, Appellant asserts that Ware’s Figure 5B embodiment—relied on by the Examiner to disclose the recited “command router”—does not disclose the recited “chip-select signal.” Br. 8–9. Appellant also contends that Ware’s Figure 6A embodiment—relied on by the Examiner to disclose the “chip-select signal”—does not disclose the “command router” limitation. *Id.* at 10. Appellant asserts further that the rejection is erroneous because it fails to explain how Ware’s embodiments “might be modified to use chip-select signals in the manner of claim 2.” *Id.*

For the following reasons, these arguments are unpersuasive of reversible error in the rejection. First, Appellant’s arguments that Figures 5B and 6A do not individually disclose certain claim limitations lack persuasive merit because those arguments do not address the rejection that was made by the Examiner. Here, the Examiner does not rely on Figure 5B

for the “chip-select signal,” but, rather, notes that limitation is disclosed in Figure 6A. Final Act. 4–5. Similarly, the Examiner relies on Figure 5B for the “command router” limitation, not Figure 6A as argued by Appellant. *Id.* at 5–6.

We are furthermore unpersuaded by Appellant’s argument that the Examiner failed to adequately explain how it would have been obvious for the skilled artisan to modify the embodiment of Figure 5B with the chip-select signal illustrated in Figure 6A and discussed in detail in Ware’s paragraph 77. The Examiner, relying on Ware’s paragraph 77 disclosure, notes that Ware’s “individual device select lines 633a and 633b are employed to perform device selection.” Final Act. 4–5. Significantly, in addition to discussing the select lines 633a and 633b depicted in Figure 6A, Ware’s paragraph 77 also discusses the “control lines (RQ)” that are depicted in Figure 5B. Ware ¶ 77. Indeed, the Examiner points to this disclosure of Ware not only in the Final Action, but also again in the Answer, explaining how the skilled artisan would have concluded from Figure 6A and paragraph 77 “that control lines RQ in Fig. 5B would comprise control signals to select devices from dedicated service select signals 633a/633b, supplied externally and not issued from the buffer” as depicted in Figure 6A. Ans. 6–8. Appellant does not address this rationale set forth by the Examiner, i.e., no Reply Brief has been filed.

Thus, on this record, we are unpersuaded that Appellant has identified reversible error in the rejection of independent claim 2. Accordingly, we sustain the rejection of this claim, as well as claims 4 and 6–11 dependent therefrom and not separately argued. Because Appellant relies on the same deficient arguments set forth above regarding the rejection of claim 12, we

Appeal 2018-008415
Application 15/336,554

likewise sustain the Examiner's rejection of this claim, as well as claims 13–17, and 21 dependent therefrom and not separately argued.

Rejection II

Because Appellant advances only the same unpersuasive arguments for this rejection as provided for Rejection I (Br. 11), we sustain Rejection II for the same reasons as set forth above.

CONCLUSION

Rejections I and II are affirmed.

DECISION SUMMARY

Claims Rejected	35 U.S.C. §	Basis / Reference	Affirmed	Reversed
2–4, 6–17, 21	103(a)	Ware	2–4, 6–17, 21	
18–20	103(a)	Ware, Yoo	18–20	
Overall Outcome			2–4, 16–21	

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED