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PERKINS COIE LLP - Micron
PATENT-SEA
PO BOX 1247
SEATTLE, WA 98111-1247

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BEFORE
THE PATENT TRIAL AND APPEAL BOARD

Ex parte KYLE K. KIRBY,[1]
Kunal R. Parekh, Philip J. Ireland, and Sarah A. Niroumand

Appeal 2018-007703
Application 15/133,121
Technology Center 2800

Before ROMULO H. DELMENDO, MARK NAGUMO, and JAMES C. HOUSEL, *Administrative Patent Judges*.

NAGUMO, *Administrative Patent Judge*.

DECISION ON APPEAL

Micron ("Kirby") timely appeals under 35 U.S.C. § 134(a) from the Final Rejection[2] of all pending claims 9 and 11–26. We have jurisdiction. 35 U.S.C. § 6. We reverse, and enter a new ground of rejection subject to our authority under 37 C.F.R. § 41.50(b).

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[1] The applicant under 37 C.F.R. § 1.46 (Application Data Sheet, filed 19 April 2019), and hence the appellant under 35 U.S.C. § 134, is the real party in interest, identified as Micron Technology, Inc. ("Micron") (Appeal Brief, filed 12 March 2018 ("Br."), 2).

[2] Office Action mailed 16 August 2017 ("Final Rejection"; cited as "FR").

OPINION

A. Introduction[3, 4]

The ′121 Specification explains that "[s]emiconductor dies typically include a plurality of integrated circuits, bond-pads coupled to the integrated circuits, and metal routing layers for routing electrical signals between the bond-pads and external contacts." (Spec. 1 [0003].) The subject matter on appeal relates to through-silicon vias ("TSV"), which the Specification describes as "interconnects to electrically couple the bond-pads and/or metal routing layers to external devices (e.g., a lead frame, a printed circuit board, etc." (*Id.* at 1 [0004].) TSVs are said to extend, often, completely through the dies (*id.* at [0004]), and to be placed close to one another, "such that the pitch between TSVs is very low" (*id.* at 2 [0005]). In certain embodiments, many of the inventive TSVs may be formed in the area taken up by a single prior art TSV. (Spec. 9 [0045]; Figures 11 and 12; claims 13 and 22 (Br. 14, 15, respectively.) The record indicates that such TSVs are useful for making three-dimensional integrated circuits and stacked dies, to reduce the connection distance between integrated circuit elements, leading to faster processing speeds. (Lim[5] 1 [0002].)

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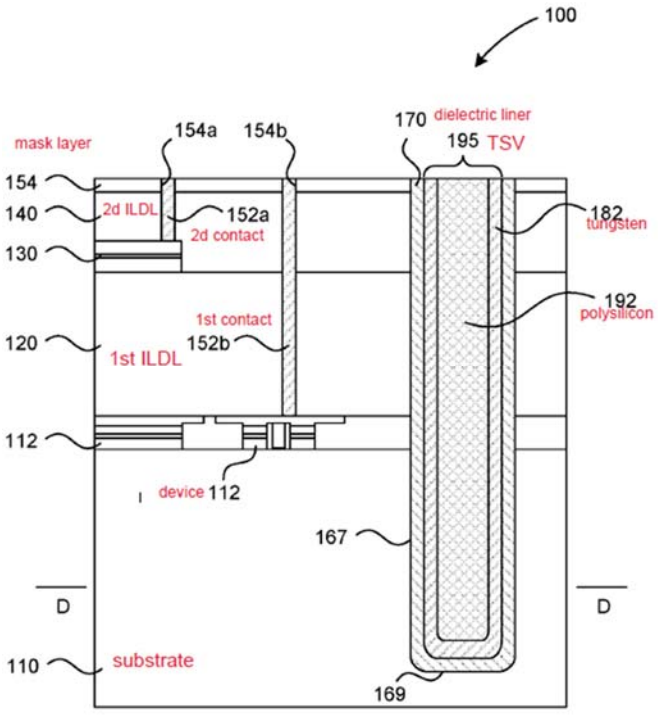
[3] Application 15/133,121, *Microelectronic devices with through-silicon vias and associated methods of manufacturing*, filed 19 April 2019, as a division of 14/144,806, filed 31 December 2013, now U.S. Patent No. 9,343,362, which is a division of 13/092,434, which was filed 22 April 2011, now U.S. Patent No. 8,753,981. The claims of the issued patents are directed to methods of manufacturing TSVs.

[4] We refer to the "′121 Specification," which we cite as "Spec."

[5] For the full citation of Lin, see n. 10, *infra*.

Manufacturing TSVs with copper is said to be difficult because the coefficient of thermal expansion for silicon differs significantly from that for copper, leading to "cracks that allow the copper to diffuse into the silicon," and to the consequent limitations on performance, particularly for small pitch sizes. (*Id.*) Moreover, it is said to be difficult to fill deep vias for TSVs with copper. (*Id.*) Tungsten (W) has been proposed as an alternative to copper, but it is said to be "impracticable to fill large TSVs with tungsten, and it is less conductive than copper." (*Id.* at [0006].) In the words of the Specification, "tungsten is not known as a ready substitute for copper in forming TSVs." (*Id.*)

{Figure 10 is shown below, with added annotations}



{Figure 10 shows a cross section of a microelectronic device wafer **100**[6]}

[6] Throughout this Opinion, for clarity, labels to elements are presented in bold font, regardless of their presentation in the original document.

Kirby seeks patent protection for a microelectronic device **100**, an embodiment of which is illustrated in Figure 10, *supra*. The device comprises electrical components **112** (e.g., transistors, switches, light emitting materials, etc. (*id.* at 6 [0033]), first (**120**) and second (**140**) electrically isolating interlayer dielectric structures (*id.* at [0034]), a first electrical contact **152b** to the electrical components, a second electrical contact **152a** (here, to metallization structure **130**) (*id.* at [0035]) , and a tungsten through-silicon via **195** comprising an outer tungsten conductor **182** and polysilicon[7] **192** within the tungsten conductor (*id.* at 7 [0039]–9 [0044]). In this embodiment, the upper surfaces of first and second contacts **152b**, **152a**, and of TSV **195** are coplanar with the upper surface of hard mask **154**. The structure shown in Figure 10 is thinned from below to line **D–D** to expose the bottom end of the TSV for electrical contact to another device.

Claim 9 is representative and reads:

> A microelectronic device [**100**], comprising:
>
> a substrate [**110**];
>
> electrical components [**112**] formed on the substrate;
>
> a first interlayer dielectric structure [**120**] over the substrate;
>
> a second interlayer dielectric structure [**140**] over the first interlayer dielectric structure;

[7] The ′121 Specification does not appear to state expressly that the polysilicon is conductive (i.e., doped). Because the purpose of the TSV is to provide a conductive link from one side of the silicon wafer to the other, we assume, without deciding, that the polysilicon is doped to be conducting, similar to the polysilicon core described by Chen at page 3 [0043]. (See n. 12, *infra*, for a complete citation.)

a first contact [**152b**]
in electrical communication with the electrical components and
extending through the first and second interlayer dielectric structures;

a second contact [**152a**]
extending through only the second interlayer dielectric structure; and

a tungsten through-silicon via (TSV) [**195**]
extending completely through the first [**120**] and second [**140**] interlayer dielectric structures and
at least partially through a thickness of the substrate [**110**],
wherein the tungsten TSV has
a tungsten conductor [**182**] and polysilicon [**192**] within the tungsten conductor,

wherein
an upper surface of first contact [**152b**],
an upper surface of the second contact [**152a**], and
an upper surface of the tungsten TSV [**195**] are all coplanar.

(Claims App., Br. 13; some formatting, bracketed labels to elements shown in Figure 10, and emphasis added.)

Remaining independent claim 19 is worded identically to claim 1 through the first wherein clause, "wherein the tungsten TSV has," and then expresses substantially the same structure; and claim 19 omits the final wherein clause reciting the coplanarity of the upper surfaces of the contacts and the TSV.

The Examiner maintains the following grounds of rejection[8, 9]:

A. Claims 9, 11, 12, 17–21, and 26 stand rejected under 35 U.S.C. § 103(a) in view of the combined teachings of Lin,[10] Chang,[11] and Chen.[12]

A1. Claims 13 and 22 stand rejected under 35 U.S.C. § 103(a) in view of the combined teachings of Lin, Chang, Chen, and Nishio.[13]

A2. Claims 14, 15, 23, and 24 stand rejected under 35 U.S.C. § 103(a) in view of the combined teachings of Lin, Chang, Chen, and Sabuncuoglu.[14]

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[8] Examiner's Answer mailed 11 May 2018 ("Ans.").

[9] Because this application claims the benefit of an application filed before 16 March 2013, the effective date of the America Invents Act, we refer to the pre-AIA version of the statute.

[10] Jing-Cheng Lin and Ku-Feng Yang, *Through-substrate vias with improved connections*, U.S. Patent Application Publication 2011/026691 A1 (3 November 2011), based on an application filed 28 April 2010.

[11] Hung-Pin Chang et al., *Via structure and via etching process of forming the same*, U.S. Patent Application Publication 2010/0244247 A1 (30 September 2010), based on an application filed 12 Mach 2010.

[12] Ming-Fu Chen and Jao Sheng Huang, *Stacked integrated chips and methods of fabrication thereof*, U.S. Patent Application Publication 2010/0178761 A1 (15 July 2010), based on an application filed 5 November 2009.

[13] Taichi Nishio et al., *Semiconductor device*, U.S. Patent Application Publication 2010/0225005 A1 (2010).

[14] Deniz Sabuncuoglu Tezcan et al., *Method for forming 3D-interconnect structures with airgaps*, U.S. Patent Application Publication 2012/0013022 A1 (19 January 2012), based on an application filed 14 July 2011, and claiming the benefit of 61/365,160, filed on 16 July 2010.

A3. Claims 16 and 25 stand rejected under 35 U.S.C. § 103(a) in view of the combined teachings of Lin, Chang Chen, and Rantala.[15]

B. Discussion

The Board's findings of fact throughout this Opinion are supported by a preponderance of the evidence of record.

Both the Examiner and Kirby treat independent claims 9 and 19 in parallel, and substantially in the same way. We therefore select claim 9 as representative. Moreover, Kirby argues only that the first and second contacts—substantively, only the second contact—are not met or rendered obvious. Kirby does not dispute the Examiner's findings or conclusions regarding the teachings of the references as to the TSV. We therefore focus our attention on the structure required by claim 9 of the first and second interlayer dielectric structures, and the first and second contacts.

The Examiner's interpretation of the term "contact" is perhaps most clearly stated in the Interview Summary attached to the Advisory Action[16]: "as far as claims of the application do not define a word 'contact' as an element comprising a single electrically conductive layer, any interconnect structure could be seen as a contact." (Adv. 3.) However, the details of the rejection are somewhat difficult to follow, due in part to seeming inconsistencies in the reading of the "first contact" and "second contact"

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[15] Juha T. Rantala et al., *Integrated circuits having organic-inorganic dielectric materials and methods for forming such integrated circuits*, U.S. Patent Application Publication 2004/0002617 A1 (2004).

[16] Advisory Action communicated 27 November 2017 ("Adv."). We cite the Interview Summary as page 3 of the Advisory.

limitations recited in the claims onto elements in Lin. Furthermore, the Examiner appears to change the identification of what elements correspond to the first and second contacts between the Final Rejection and the Examiner's Answer.

Because, as Kirby points out, and as will be discussed in more detail *infra*, the structure in Chang identified by the Examiner as a "contact" that extends through only the second interlayer dielectric structure" cannot reasonably be so characterized—and is inconsistent with other findings by the Examiner regarding the "first contact" disclosed by Chen, we reverse the rejections of record as being based on a harmfully erroneous claim interpretation.

Moreover, there appear to be further unquestioned assumptions that are not consistent with the broadest reasonable interpretation of the claims, read in light of the Specification, from the point of view of a person having ordinary skill in the art. Specifically, the Examiner finds, and Kirby does not appear to dispute, that "Lin does not teach that the second contact extends *only through* the second interlayer dielectric layer—*since his device has more than two interlayer dielectric layers*." (FR 4, ll. 4–6 (emphasis added).) In other words, the Examiner and Kirby appear to agree that the claims are limited to the two recited interlayer dielectric structures. (Ans., paragraph bridging 4–5: "[i]t is clear from Fig. 10 that the only reason this figure does not teach the claimed dispositions of the 'first and second contacts' is a number of interlayer dielectric structures **34** that exceeds two.") However, as will become apparent, the claims presented on appeal are open to additional interlayer dielectric structures. Under the proper interpretation, the subject matter of the independent claims would have been

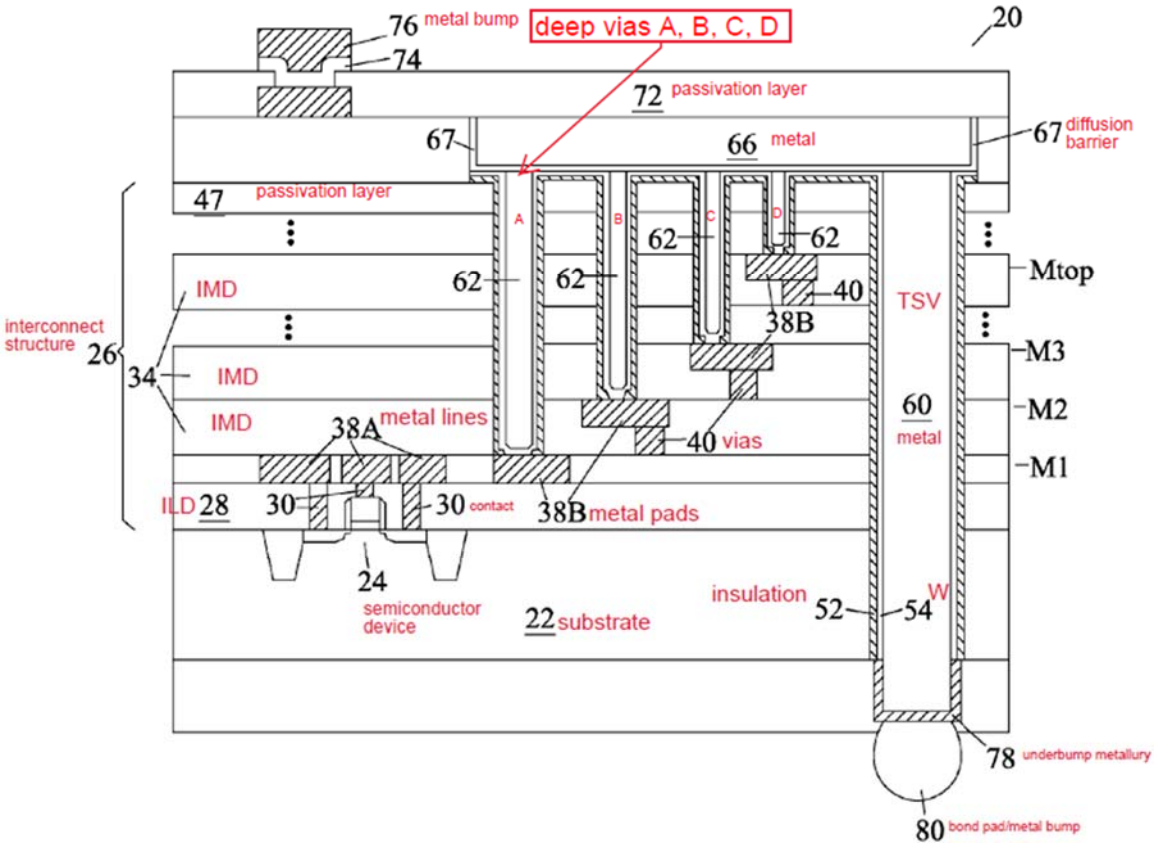
obvious in view of the combined teachings of Lin and Chen alone. We therefore enter a new ground of rejection for independent claims 9 and 19.

Briefly, the Examiner finds that Lin teaches, in Figure 10, shown on the following page, a microelectronics device that meets the limitations of claims 9 and 19 but for the recited first contact (FR 4, ll. 1–4), the second contact (*id.* at 4–6), and but for a tungsten TSV having a tungsten conductor and polysilicon within the tungsten conductor (*id.* at ll. 6–7).

More specifically, the Examiner finds that Lin teaches: a substrate **22** (*id.* at 3, 1st bullet); electrical components **24** (*id.* at 2d bullet); a first interlayer dielectric structure (in which metallization **M2** is formed) (*id.* at 3rd bullet) ; a second interlayer dielectric structure (in which metallization **M3** is formed) (*id.* at 4th bullet); "room" for creating a first contact with electrical components **24** (*id.* at 5th bullet), a second contact **54**/**62** in opening **46A**[17] (*id.* at 6th bullet); a tungsten TSV **54**, **60** (*id.* at 7th bullet), but not one with polysilicon within the tungsten (*id.* at 4, ll. 7–8); and that the upper surfaces of the second contact and the TSV are coplanar (*id.* at 3, last bullet).

[17] Opening **46A** is shown in Figures 4–6 (not reproduced here), and indicated in annotated Lin Figure 10, *infra*, by the label "**A**.".

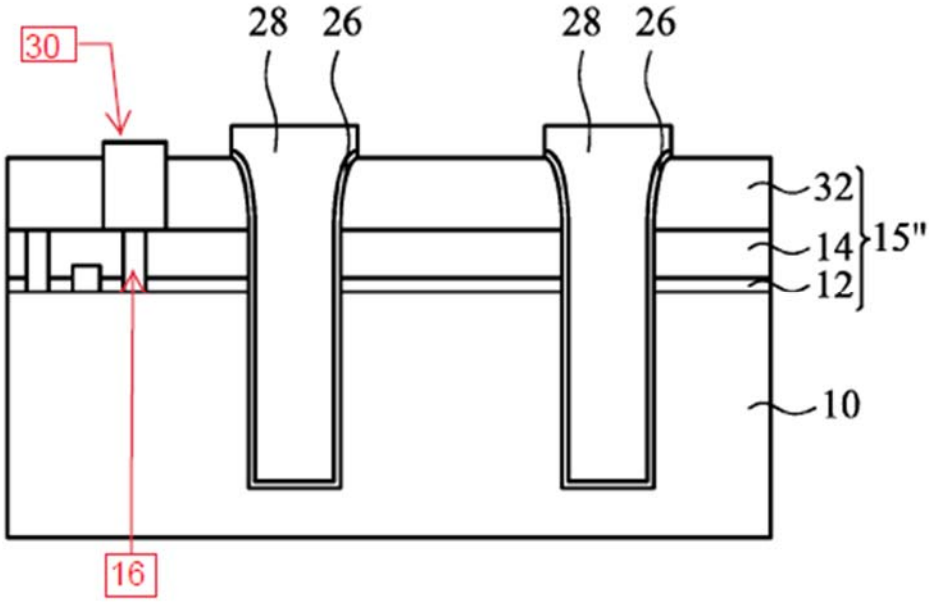
{Lin Figure 10 (annotated) is shown below}



{Lin Figure 10 shows a cross section of a wafer comprising TSV (**60**), deep conductive vias **62**, **A**–**D**), and semiconductor device **24**. (We have used the terms used by Lin, rather than the labels applied by the Examiner.)}

The Examiner finds the structure taught by Lin differs from the claimed structure in that: (1) Lin does not teach explicitly an electrical communication with the electrical components, and, thus, does not teach coplanarity with the upper surfaces of the second contact and the TSV. (FR 4, ll. 1–4.) (2) Lin does not teach that the second contact extends through only the second interlayer dielectric structure, because Lin's device has more than two interlayer dielectric layers. (*Id.* at ll. 4–6.) (3) Lin does not teach a tungsten TSV having polysilicon within the tungsten conductor. (*Id.* at ll. 6–7.)

The Examiner finds that Chang describes, in Figure 13, shown below,

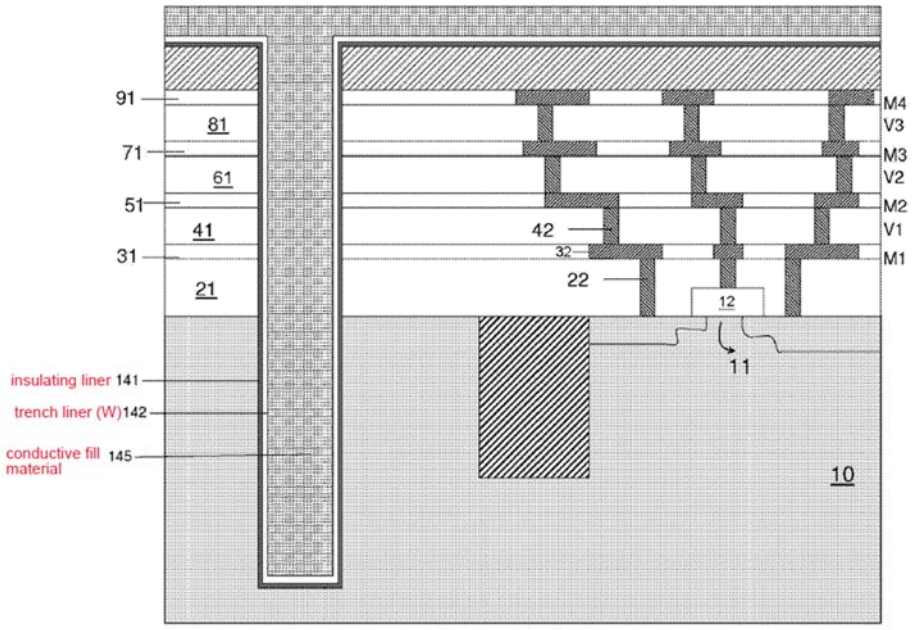


{Chang Figure 13 shows a cross section of a device with TSVs filed with polysilicon conductor **28**; annotations added}

a microelectronics device similar to that described by Lin, but comprising only first and second interlayer dielectric structures **14** and **32**. (*Id.* at 4, ll. 8–9.) The Examiner finds further that Chang discloses a "second contact" **30** that extends only through second interlayer dielectric structure **32**. (*Id.* at ll. 10–11.)

The Examiner finds that Chen discloses "a first contact (made of multiple electrically conductive parts **22**, **32**, **42** in interlayer dielectric structures **31**/**21**, **41**/**51**, **61**/**71**, **81**/**91**) . . . in electrical communication with electrical components **12** and extending through the first and second interlayer dielectric structures (**21**/**31** and **41**/**51**, correspondingly." (FR 5, 3rd bullet.) The Examiner finds further that Chen describes a TSV comprising a conductor that may be tungsten (trench liner **142**) having a conductive filler material **145** that may be polysilicon. (*Id.* at 4th & 5th bullets.) These structures are shown in Chen, Figure 1G, on the next page.

{Chen Figure 1G is shown below}



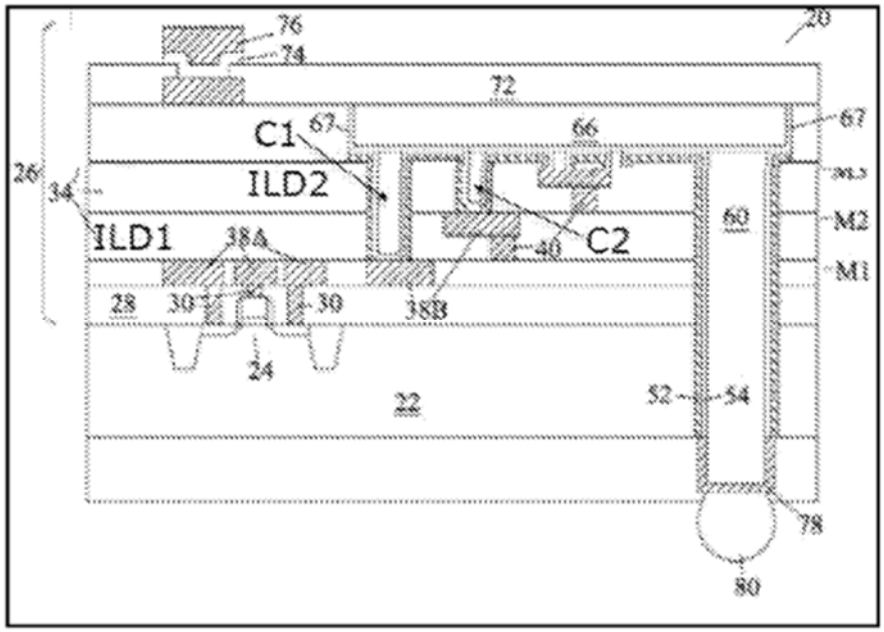
{Chen Figure 1G shows a cross section of a device with a TSV (left); tungsten liner **142** and conductive filler **145** that may be polysilicon) and contacts **42-32-33** in dielectric layers **51**/**41**, **31**/**21**, to device **12** (right); annotations added}

The Examiner concludes it would have been obvious to modify Lin by providing only metallization layers **M1**–**M3**, because thinner devices are desired in the semiconductor industry. (FR, sentence bridging 4–5.) The Examiner finds that the second contact (**54**, **62** in via **A**, *supra*) would extend only through the second interlayer dielectric layer. The Examiner concludes further that creating a first contact with Lin's electrical component **24** would have been obvious in view of Chen (*id.* at 10, last para.), as would the use of a tungsten TSV with polysilicon within the tungsten (*id.* at 11, first para.).

Kirby argues that Lin does not disclose or suggest a second contact extending through only a second interlayer dielectric structure. (Br., para. bridging 5–6.) Kirby argues further that it is improper to identify Chang's interconnect structure **30** and intermetal dielectric layer **32** as single layers,

because Chang discloses these labeled structures as explicitly including multiple layers. (*id.* at 6.) Kirby urges further that it is improper, even accepting Chang layer **32** as a single layer, to ignore the additional portion of the connect structure **16** that passes through dielectric layer **14** and etch stop layer **12**. (*Id.* at 7.) The additional connect structures, Kirby urges, provide the electrical coupling between interconnect structure **30** and front-end-of-line features formed on the front surface of the semiconductor substrate, i.e., below dielectric layer **14** in Chang, Figure 13, *supra*. Thus, they "should also be understood as a part of the same interconnect structure." (*Id.* at sentence bridging 7–8.)

The Examiner responds that the main reason for combining Chang and Lin is that Chang discloses only two interlayer dielectric layers, namely **32** and **14**, while describing a similar device with similar structures. (Ans. 8, 1st para.) The Examiner also provides an annotated Lin Figure 10, modified in view of Chang (Ans. 9), which is reproduced below.



{Annotated Lin Figure 10, modified by the Examiner in view of Chang}

Kirby did not file a Reply Brief.

In annotated modified Lin Figure 10, the Examiner identifies: the first interlayer dielectric structure as layer **M1** (containing metal pad **38B** and metal lines **38A**, which, through metal contacts **30** in layer **M1**, make contact with the source and drain of transistor **24** in interlayer dielectric layer **28**); the second interlayer dielectric structure as layer **M2** (containing metallization pad **38B** and via **40**); the first contact as the via formed in opening **A**; and the second contact as the via formed in opening **B**. (Ans. 8–9.)

There are two major difficulties with this interpretation.

First, procedurally, this interpretation differs substantively from the rejection set out in the Final Rejection and adhered to in the Advisory Action. Specifically, the Examiner never expressly identified which structure was thought to correspond to the "first contact"; but the Examiner identified clearly, for both claim 1 (FR 3, 6th bullet), and again for claim 19 (*id.* at 8, 6th bullet), the leftmost deep via, formed in opening **A**, as the "second contact." While we do not have jurisdiction over this procedural matter, which in any event Kirby has not objected to, we observe that such lapses tend to detract from the clarity of the record, and tend to increase needlessly the burden on the applicant for patent, as well as on the PTO, both at the PTAB, and, ultimately, on the Examiner.

Second, substantively, the Examiner does not provide a reasonable explanation, supported by the preponderance of the evidence of record, for the dissection of electrical contact structures that form connections to the electrical components. Indeed, the Examiner's conclusion that "any

interconnect structure could be seen as a contact" (Adv. 3) better supports Kirby's arguments that the "contacts" described by Chang cannot be dissected into an electrically conductive interconnect structure **30** and a second electrically conductive "contact structure **16** [which] is formed in a contact opening penetrating the contact etch stop layer **12** and the ILD layer **14** to provide electrical contact to the device **100**." (Chang 2 [0012], ll. 22–14.) Indeed, the Examiner's definition of the term "contact" describes the full interconnect structure described in Chen, Figure 1G, described *supra*. Absent some indication in the ′121 Specification that such a dissection is contemplated for some "contact" in the claimed invention, the Examiner's broad interpretation is not reasonable.

The Examiner has not directed our attention to such an indication, and we therefore conclude, on the present record, that the Examiner's interpretation, as applied to the references, results in harmful error. In particular, pads **38B**, which "land" subsequently formed deep vias **A**–**D** (Lin 1 [0014], last sentence), are part of the "contact," which includes the conductive deep vias, cause the contact identified by the Examiner as the "second contact" in annotated Lin Figure 10 to extend through not only the "second interlayer dielectric structure" **ILD2**/**M2**, but also through "first interlayer dielectric structure" **ILD1**/**M1**. Thus, the interpretation proffered by the Examiner is harmfully erroneous.

Closer inspection of the language of claim 9, however, in the context of the disclosure, indicates that the Examiner has interpreted the phrase "a second contact extending *through only* the second interlayer electric structure" (Claims App., Br. 13, emphasis added) too narrowly.
Lin Figure 10, reproduced *supra* at 3, shows contact **152a**, contact **152b**, and

TSV **195** each extending through mask layer **154**. Mask layer **154** does not appear to be a functional equivalent of the interlayer dielectric layers,[18] and thus it does not appear to be reasonable to lump it as part of the second ILD. Thus, the words "through only" should be read as "through, but no further than" the second interlayer dielectric structure. On the other hand, reading the term "through only" as excluding layers above the second ILD would cause the claim to lack written description in the Specification. Moreover, our interpretation of the phrase "through only" gives substance to the transitional phrase "comprising" by allowing the presence of structures and materials not recited in the claim (that are not inconsistent with the express limitations recited in the claims). While other interpretations should not be foreclosed during examination, the evidentiary findings and factual inquiries for those conclusions have not been conducted, and we decline to consider them in the first instance. Our primary function is review, not examination in the first instance.

In any event, both original Lin Figure 10 and the Examiner's annotated Lin Figure 10 display features that, with the teachings of Lin and of Chen, would have rendered the claimed subject matter obvious. In particular, Lin teaches that "[t]he metal features in interconnect structure **26** may be electrically coupled to semiconductor devices **24**." (Lin 1 [0014], ll. 11–13.) Applying the reading of "contact" urged by Kirby—which we

[18] We understand, without deciding, based on the exchanges between the Examiner and Kirby, that the terms "interlayer dielectrics" and "interlayer metal dielectrics" are essentially interchangeable with one another and with the term "interlayer dielectric structure" used in Kirby's Specification and claims.

adopt as our own—any of deep vias **A**–**D**, if electrically connected to device **24** by conductive paths, would comprise a contact "extending through the first and second interlayer dielectric devices." There are no further limits on the first contact. Although the contact **B** in original Figure 10 (and in the Examiner's Annotated Figure 10, labeled as **C2**) extend through interlayer dielectric layer **1**, and thus are excluded from the recited "second contact," claim 9 does not exclude such a structure, due to the transitional phrase "comprising." Contact **C** in original Lin Figure 10, and the right-most contact in the Examiner's Annotated Lin Figure 10, if not connected to device **24** through the intervening interlayer dielectric layers, meet the limitation that the "second contact" extends "through only the second inter-layer dielectric structure." In this regard, it should be noted that claim 9 does not state to what the second contact must be connected. Contact **D**, like contact **B**, is not excluded from claim 1 due to the presence of the open transitional phrase, "comprising."

Substituting one form of TSV for another, would have been obvious, absent evidence that a particular potential substitute TSV would have been expected to be incompatible with the environment of the reference TSV. No such arguments have been raised by Kirby. On the present record, we hold that independent claims 9 and 19 would have been obvious, and hence are unpatentable in view of the combined teachings of Lin and Chen. Because the Examiner's modification of Lin in view of the teachings of Chang and Chen contain structures that meet the limitations of claims 9 and 19, properly interpreted, we hold those claims obvious in view of the teachings of Lin, Chang, Chen.

Because the dependent claims appear to involve only the TSV,[19] and have not been contested, we also reject the dependent claims over the further combinations of references relied on by the Examiner.

Because we have relied on a claim interpretation different from that of the Examiner, and because we cannot characterize the Examiner's errors as "harmless," we denominate the rejections as new grounds of rejection.

C. Conclusion

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
9, 11, 12, 17–21, 26	103	Lin, Chang, and Chen		9, 11, 12, 17–21, 26
13, 22	103	Lin, Chang, and Chen, and Nishio		13, 22
14, 15, 23, 24	103	Lin, Chang, Chen, and Sabuncuoglu.		14, 15, 23, 24
16 , 25	103	Lin, Chang, Chen, and Rantala		16 , 25
Overall Outcome				9, 11–26

[19] Claim 12, which depends from claim 9, recites that "the substrate comprises a semiconductor material." We understand, without deciding, that the word "silicon" in the term "through silicon via," is recognized in the art as a historical artifact, rather than a requirement that the substrate comprise silicon.

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
New Ground of Rejection				
9, 11–26	103	Lin, Chen or Lin, Chang, and Chen		
13, 22	103	Lin, Chen, and Nishio, or Lin, Chang, Chen, and Nishio		
14, 15, 23, 24	103	Lin, Chen, and Sabuncuoglu, or Lin, Chang, Chen, and Sabuncuoglu		
16 , 25	103	Lin, Chang, Chen, and Rantala, or Lin, Chang, Chen, and Rantala		

This decision contains a new ground of rejection.

37 C.F.R. § 41.52(a)(1) provides that "Appellant may file a single request for rehearing within two months of the date of the original decision of the Board." 37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review." 37 C.F.R. § 41.50(b) also provides that Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which

event the proceeding will be remanded to the examiner. . . .

(2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

REVERSED
37 C.F.R. § 41.50(b)