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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JOHN KALAMATIANOS, PAUL KELTCHER, MARIUS EVERS, and CHITRESH NARASIMHAIAH

Appeal 2018-007676
Application 13/944,148
Technology Center 2100

Before MAHSHID D. SAADAT, JOHNNY A. KUMAR, and JOHN A. EVANS, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–4, 6–10, 12–18, and 20, which are all the claims pending in this application.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a) (2017). Appellant identifies the real party in interest as Advanced Micro Devices, Inc. Appeal Br. 1.

[2] Claims 5, 11, and 19 have been canceled.

STATEMENT OF THE CASE

Introduction

Appellant's disclosure is directed to methods of improving processing efficiency of a prefetcher for moving data expected to be demanded by an executing program thread to a cache, whereby the prefetcher analyzes memory access requests ("demand requests") by the executing program thread to identify patterns in the memory addresses of the demand requests by identifying the data that is expected to be demanded. Additionally, the physical addresses are typically organized into memory pages to facilitate efficient memory access. However, the problem with conventional prefetchers is their inability to properly identify memory access patterns for strides that cross memory page boundaries system because sequential addresses in the virtual address space can refer to non-sequential memory pages in the physical address space. *See* Spec. ¶¶ 2–3.

Claim 1 is illustrative of the invention and reads as follows:

> 1. A method comprising:
>
> identifying, at a processor, a first stride value based on a first memory access request to a first memory page;
>
> in response to a sum of the first stride value and a physical memory address of the first memory access exceeding a page boundary of the first memory page, maintaining a first prefetch confidence associated with the first memory access; and
>
> in response to a second memory access to a second memory page subsequent to the first memory access:
>
> identifying an offset portion of the physical memory address of the first memory access;
>
> identifying a sum value equal to a sum of the offset portion of the physical memory address of the first memory access and the first stride value;

> in response to the sum value matching an offset portion of a second physical memory address of the second memory access, matching a second stride value for the second memory access to the first stride value; and
>
> prefetching data from a memory based on the maintained first prefetch confidence in response to the second stride value matching the first stride value.

Appeal Br. 13. (Claims App.).

The Examiner's Rejections

Claims 1–4, 6, 9, 10, 15–18, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rowlands (US 2014/0149679 A1; pub. May 29, 2014) and Assarpour (US 2014/0086241A1; pub. Mar. 27, 2014). Final Act. 2–19.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rowlands, Assarpour, and Chan (US 4,722,047; iss. Jan. 26, 1988). Final Act. 19–20.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rowlands, Assarpour, and Ramani-Augustin (US 2014/0006718 A1; pub. Jan. 2, 2014). Final Act. 20–22.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rowlands, Assarpour, and Kou (US 2012/0254540 A1; pub. Oct. 4, 2012). Final Act. 22–23.

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rowlands, Assarpour, Kou, and Gonin (US 2006/0004996 A1; pub. Jan. 5, 2006). Final Act. 22–28.

ANALYSIS

Claim Rejection over Rowlands and Assarpour

The Examiner finds Rowlands discloses the recited method steps for identifying a first stride, maintaining a first prefetch confidence in response to a sum of the first stride value and a physical memory address of the first memory access exceeding a page boundary of the first memory page, and prefetching data from a memory in response to a second memory access to a second memory page. Final Act. 2–4 (citing Rowlands Figs. 1, 2A, 2B, 6; ¶¶ 41, 43, 48, 65, 67, 77). The Examiner relies on Assarpour as disclosing "identifying an offset portion of the physical memory address of the first memory access;" "identifying a sum value equal to a sum of the offset portion of the physical memory address of the first memory access and the first stride value;" and "in response to the sum value matching an offset portion of a second physical memory address of the second memory access, matching a second stride value for the second memory access to the first stride value." Final Act. 5 (citing Assarpour ¶¶ 27–29). The Examiner justifies the combination as assuring "that memory is readily accessible in that the offset and the stride allow the system to access desirable data within the memory (*see* Assarpour: [0028]–[0029])." *Id.*

Appellant contends the rejection of claim 1 is in error because the cited portions of Assarpour in paragraphs 27–29 do not teach "memory addresses having an offset portion and summing a stride value to the offset portion in response to crossing memory page boundaries." Appeal Br. 6. Appellant further argues Assarpour's discussion of the entry stride and the memory addresses indicates:

> Accordingly, Assarpour only discusses stride in the context of a value representing differences in the physical addresses

> between sequential entries in a single physical table, and is irrelevant towards claim l's determining of whether a pattern of memory access requests continues when exceeding page boundaries (i.e., determining whether stride between addresses of memory access requests stays the same).

Appeal Br. 7. According to Appellant, Assarpour "only discusses offsets in the context of a value representing the differences between the base address of a physical table and the addresses of entries in the physical tables," and not "summing a stride value to the offset [portion of the physical memory address] when crossing memory page boundaries." Appeal Br. 8.

The Examiner responds by explaining:

> As seen in the Final Office Action (10/19/2016), Assarpour discloses identifying an offset portion of the physical memory address of the first memory access [[0027]–[0029]], and identifying a sum value equal to a sum of the offset portion of the physical memory address of the first memory access and the first stride value [[0028], where adding to the current offset means a sum value is identified], *while Rowlands discloses in response to a sum of the first stride value and a physical memory address of the first memory access exceeding a page boundary of the first memory page* [[0065] "the confidence level can continue to change (e.g., increase) if the pattern of access requests continues across the second physical memory page 402", thus the pattern (as seen in Table 1), from which the stride value is derived, continues across the second memory page; *the memory page crossing occurring by the sum of the stride, such as the first stride value* ("2" in Table 1), *and the memory address of a memory access*, such as the first memory access, exceeding the page boundary of the first memory page and continuing onto the second memory page].

Ans. 14 (emphases added). The Examiner further finds "Rowlands is relied upon to teach crossing the page boundary while Assarpour is relied upon to teach identifying an offset and summing as seen above." Ans. 15. The

Examiner explains Appellant's arguments are directed to the references separately whereas the rejection is based on the combination of Rowlands and Assarpour. Ans. 16.

Based on a review of Rowlands, we find the cited paragraph 65 relates to prefetching by using the confidence level and the first prefetch distance for a second prefetch. Rowlands ¶ 65. The reference further teaches "[t]he second prefetch distance and the confidence level can continue to change (e.g. increase) if the pattern of access requests continues across the second physical memory page 402." *Id.* Rowlands refers to the process in the flowchart of Figure 5 for situations where "the access requests continue until the prefetch distance again extends to or beyond the boundary of the second physical memory page 402." *Id.*

As argued by Appellant (Reply Br. 2), the cited portions of Rowlands and Assarpour separately discuss fulfilling a request across a page boundary of the memory and adding the stride value to the physical address respectively, the proposed combination does not teach or suggest "identifying an offset portion of a first physical memory address, adding the offset portion to a stride value, and determining whether the sum matches an offset portion of a second physical memory address on a different memory page." It is not apparent, and the Examiner does not clearly explain, how combining Rowlands and Assarpour would result in "memory addresses having an offset portion and summing a stride value to the offset portion when crossing memory page boundaries. *See e.g.*, *Appeal Brief*, pp. 6–8." *Id.* We also agree with Appellant that "Assarpour only discusses offset in the context of a value that is added to the base address of a physical table to access entries within the physical table. *See e.g.*, *Appeal Brief*, p. 7.

However, Assarpour provides no disclosure that such offsets are a different portion (i.e., bits) of the physical address." Reply Br. 5. In other words, neither references compare the sum of the first stride and the offset portion of a physical memory address with the page boundary of the first memory page.

For the above reasons, we agree with Appellant that the Examiner's proposed combination does not teach or suggest the disputed limitations of claim 1, nor of other independent claims which recited similar features. Therefore, Appellant's arguments have persuaded us of error in the Examiner's position with respect to the rejections of independent claims 1, 9, and 15, as well as claims 2–4, 6, 10, 16–18, and 20 dependent therefrom.

Claim Rejection over Rowlands and Assarpour in view of other Applied Prior Art

The Examiner's application of the remaining references does not make up for the above-discussed deficiency in the combination of Rowlands and Assarpour. *See* Final Act. 19–28. Accordingly, for the same reasons stated above, we are persuaded of Examiner error in rejecting claims 7, 8, and 12–14.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Basis	Affirmed	Reversed
1–4, 6, 9, 10, 15–18, 20	103	Rowlands, Assarpour		1–4, 6, 9, 10, 15–18, 20
7	103	Rowlands, Assarpour, Chan		7
8	103	Rowlands, Assarpour, Ramani-Augustin		8

12	103	Rowlands, Assarpour, Kou		12
13, 14	103	Rowlands, Assarpour, Kou, Gonion		13, 14
Overall Outcome				1–4, 6–10, 12–18, 20

REVERSED