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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JOHN COLGROVE and ETHAN L. MILLER

Appeal 2018-007306
Application 14/563,214
Technology Center 2100

Before MICHAEL J. STRAUSS, ADAM J. PYONIN, and DAVID J. CUTITTA II, *Administrative Patent Judges.*

STRAUSS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–20. Final Act. 1. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.[2]

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Pure Storage, Inc. App. Br. 2.

[2] We refer to the Specification, filed December 8, 2014 as amended on July 25, 2016 ("Spec."); the Final Office Action, mailed February 16, 2018 ("Final Act."); Appeal Brief, filed April 30, 2018 ("App. Br."); Examiner's

CLAIMED SUBJECT MATTER

The claims are directed to an interface for solid-state storage devices. Spec., Title. Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A system comprising:
>
> one or more storage devices that each comprise a respective processor configured for storage device management; and
>
> a storage controller coupled to each of the one or more storage devices, wherein the storage controller is configured to:
>
> notify a storage device of the one or more storage devices that the storage controller is taking control of the storage device in response to detecting one or more conditions of a performance of the first replaceable[3] storage device;
>
> switch, in response to the detecting the one or more conditions of the performance of the storage device, control over storage device management from the respective processor for the storage device to the storage controller; and
>
> place the processor of the storage device in an idle state.

REFERENCES[4]

The prior art relied upon by the Examiner is:

Dillow et al.	US 2012/0036309 A1	Feb. 9, 2012
Batwara et al.	US 2013/0166855 A1	June 27, 2013
Goss et al.	US 2014/0115233 A1	Apr. 24, 2014
Shaharabany et al.	US 2015/0178194 A1	June 25, 2015
Chen et al.	US 2015/0212938 Al	July 30, 2015

Answer, mailed June 28, 2018 ("Ans."); and Reply Brief, filed July 11, 2018 ("Reply Br.").

[3] Should prosecution be continued, claim 1 should be amended to address a lack of antecedent basis for the recited *first replaceable* storage device.

[4] All citations herein to these references are by reference to the first named inventor only.

REJECTIONS

Claims 1–3, 8–10, and 15–17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen and Dillow. Final Act. 3–11.

Claims 4, 7, 11, 14, and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen, Dillow, and Batwara. Final Act. 11–13.

Claims 5, 12, and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen, Dillow, Batwara, and Goss. Final Act. 13–16.

Claims 6, 13, and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen, Dillow, Batwara, and Shaharabany. Final Act. 16–17.

ANALYSIS

Appellant's contentions are unpersuasive of reversible Examiner error. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken (Final Act. 2–17) and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellant's Appeal Brief (Ans. 3–7) and concur with the conclusions reached by the Examiner. We highlight the following for emphasis.

Notification Limitation

Claim 1 recites a storage controller configured to notify a storage device of the one or more storage devices that the storage controller is taking control of the storage device in response to detecting one or more conditions of a performance of the first replaceable[5] storage device (the "notification" limitation). Although admitting that Chen "in isolation" fails to teach the notification limitation, the Examiner finds the limitation is taught by the

[5] *See* fn. 3, *supra*.

combination of Chen and Dillow. Final Act. 4–5. In connection with Chen, the Examiner finds the reference teaches garbage collection can be performed locally by each data storage device (DSD) in a first mode or globally by garbage collection manager 10 of host 101 across multiple DSDs in a host-controlled second mode. *Id.* The Examiner finds Dillow's disclosure of an O-RAID controller informing devices of parameters for scheduling or forcing garbage collection teaches providing notification that the O-RAID controller is taking control of garbage collection activities. *Id.* at 5–6.

Appellant contends Dillow only coordinates garbage collection activities of storage devices but does not take control. App. Br. 6–9. "[I]t logically follows that Dillow also fails to teach or suggest a storage controller notifying a processor of a storage device that the storage controller is taking control of the storage device." *Id.* at 7. Appellant further argues the Examiner improperly takes official notice in finding "[i]n the embodiment where the O-RAID controller informs the devices of time or limits, the act of informing them would necessarily also notify them that the O-RAID controller is taking control of garbage collection activities." *Id.* at 9 (citing Final Act. at 6) (underlining omitted).

The Examiner responds, explaining that, although neither Chen nor Dillow individually teach the disputed notification limitation, the limitation is taught by their combination. Ans. 4.

> Dillow's disclosure has been relied upon to disclose the following: the use of state information to have a global controller to schedule and force garbage collection on storage devices. Using this disclosure, the modification is proposed where either Chen's host or DSD processors perform garbage collection (based on the disclosure of Chen providing exclusive modes),

> and the state information being used to schedule and force host garbage collection would force a switch. As part of this, scheduling and forcing the garbage collection the host controller would require a notification from the host to DSD controllers.

Id. at 4–5.

Appellant replies, arguing "there is no teaching or suggestion that the O-RAID controller 'necessarily' notifies an SSD controller that the O-RAID controller is 'taking control' because the O-RAID controller does not take control of the SSD." Reply Br. 10 (underlining omitted). According to Appellant, instead of notifying the SSD has taken control, the "O-RAID controller informs the SSD—as part of globally coordinating garbage collection across all of the multiple SSDs—of when to schedule garbage collection so as not to have the performance impact that would occur if all SSDs performed garbage collection at the same or similar times." *Id.* Appellant further argues it is improper to take official notice that garbage collection includes providing notification because such notification is not well known in the prior art. *Id.* (citing MPEP § 2144.03).

Appellant's arguments are not persuasive of reversible Examiner error. Appellant fails to explain why the claimed notification is distinguishable over Dillow's O-RAID controller's scheduling of or forcing devices to perform garbage collection. Providing a schedule directing the operation of a device and/or forcing a device to perform a function, i.e., exercising control, under a broad but reasonable interpretation, also teaches notifying the device being controlled that control is being exercised. Such an interpretation is consistent with Appellant's Specification disclosing that a "storage controller may send a command to the storage device notifying the storage device that the storage controller is taking over as the main

controller of the storage device (block 810). As the main controller of the storage device, the storage controller may . . . determine when to erase individual erase blocks, . . . and perform one or more other functions." Spec. ¶ 82 (cited by Appellant for disclosing the disputed notification limitation. *See* App. Br. 4). Furthermore, contrary to Appellant's argument, exercising control for the purpose of coordinating activities between or among devices is nonetheless controlling the devices and controlling the devices is, in and of itself, notifying the device of taking control.

We also disagree with Appellant's argument the Examiner improperly took official notice that garbage collection includes providing notification because such notification is not well known in the prior art. Reply Br. 10. Instead, as explained by the Examiner, "official notice has not been taken" (Ans. 6); rather, the Examiner provides reasons why scheduling and forcing garbage collection requires the host controller notify the DSD controllers. That is, to schedule or force garbage collection, one skilled in the art would have understood the schedule or command forcing garbage collection must be communicated to the DSD controllers, thereby notifying the DSD controllers of control by the host. This is simple logic and reasoning, not official notice.

Control Switching Limitation

Claim 1 recites the storage controller is further configured to switch, in response to the detecting the one or more conditions of the performance of the storage device, control over storage device management from the respective processor for the storage device to the storage controller (the "switching" limitation). As in the case of the notification limitation, the Examiner finds "Chen fails to teach[,] in isolation[,] where the storage

controller is configured [to perform the switching limitation]." Final Act. 4. The Examiner combines Chen's host controlled and DSD controlled modes of garbage collection with Dillow's selective use of (i) individual and (ii) globally coordinated garbage collection responsive to state information for teaching or suggesting the disputed switching limitation. *Id.* at 5–6.

Appellant contends "using state information as an indicator to switch between modes—has no basis at all in the cited portions of Chen or Dillow." App. Br. 12 (underlining omitted). Appellant further argues, although responsive to garbage scheduling from the storage controller, "the storage device processer never gives up control to a storage controller." *Id.* at 13. In particular, according to Appellant:

> [W]hile the cited host controller notifies a storage device of when to schedule garbage collection (to avoid multiple storage devices to perform garbage collection at a same time), there is no teaching or suggestion of a host controller using state information to "switch modes," much less using "state information" as a basis for a storage controller switching control of storage device management from a storage device processor to the storage controller.

Id. (underlining omitted).

The Examiner responds, contending Appellant fails to address the combination of references as applied. Ans. 5. The Examiner explains "Chen has been relied on to teach a mode where a storage controller controls device storage management and a mode where a storage device controls storage management, with Dillow teaching the ability to switch between modes based on operating conditions." *Id.* The Examiner further disagrees the references fail to teach switching modes based on state information:

> The citation to Dillow in page 6 of the [Final Act.] provides a clear citation where state information is used to determine an

> appropriate time to initiate a global garbage collection. The obviousness analysis follows with how one of ordinary skill in the art could utilize state information to switch between modes; in Dillow, this is whether the individual devices control garbage collection; in Chen, the analysis follows from the modification proposed to utilize the host or device controlled modes.

Id.

Appellant's argument is unpersuasive of reversible Examiner error.

Contrary to Appellant's argument, the prior art discloses

> State information useful for determining the need for a [garbage collection] cycle may include, but is not limited to:
> [(a)] Internal fragmentation level . . . ;
> [(b)] Number of free erase blocks . . . ;
> [(c)] ECC (error correction code) correctable error rate . . . ;
> [and] . . .
> [(d)] [P]oints in the I/O stream that are expected to have extended idle periods, and initiates a [global garbage collection] cycle during those lulls in activity.

Dillow ¶¶ 44–48. We note such state information (d), including idle periods (i.e., a condition), appears to be particularly relevant to the problem to which Appellant's application is directed.

> Garbage collection operations are typically performed in the background by the storage device in between the servicing of memory operations. However, the storage controller does not have visibility into when the storage device is performing garbage collection operations, and consequently, the storage controller may inadvertently schedule operations to the storage device at inopportune times.

Spec. ¶ 6.

> [S]torage controller 310 may initiate garbage collection operations in response to determining that the system is sufficiently idle and/or in response to detecting one or more other conditions.

Spec. ¶ 51. Similar to Dillow, Chen also discloses attributes of states (i.e., conditions) relevant to managing data storage devices. "The availability of the source or destination portions may also be considered. In such an example, host 101 may define an attribute based on an availability of the source or destination portions so that there is less activity or operations being performed at the source or destination portions." Chen ¶ 59. Thus, the prior art teaches or suggests criteria defining states triggering global garbage collection.

We note the disputed limitation does not require control be transferred exclusively to the storage controller and away from the storage device processor such that initiation and control of device operations including garbage collection by the storage device processor are inhibited. Even so, as found by the Examiner,

> Chen discloses that garbage collection "can be performed by either host 101 or by a DSD", [0048], see also "GC manager 10 may reside at each of DSDs 106, 107, 108, and 109 so as to distribute execution of GC manager 10 throughout system 100", [0025]. As understood, in one embodiment, the host controls garbage collection, or storage device management, and in another embodiment, the individual DSD's do.

Final Act. 4. The Examiner further finds "Chen's disclosure of the two embodiments are interpreted to be exclusive to one another; the language says either the host or the DSD performs garbage collection." *Id.* Therefore, under a broad but reasonable interpretation of the disputed switching limitation, because the prior art teaches locally initiated garbage collection and, in the alternative, globally initiated garbage collection, the prior art teaches or suggests switching control over storage device management from the respective processor for the storage device to the

storage controller.

Idle State Limitation

Claim 1 further recites the storage controller is configured to place the processor of the storage device in an idle state (the "idle" limitation). The Examiner finds Chen discloses garbage collection is performed either locally by the DSD or, in the alternative, is performed globally by the host controller. Final Act. 4. "Necessarily, when the host is performing garbage collection, the processors found on the DSDs are not performing garbage collection and would be idle." *Id.* Appellant argues Chen's processor is not necessarily idle if it is not performing garbage collection. App. Br. 17. According to Appellant, because Chen "describes data storage processors performing operations when not performing garbage collection" (*id.* at 18), switching control of garbage collection from the data storage processor to the storage device does not place the processor of the storage device in an idle state. *Id.* The Examiner responds "as processors can be active or idle at different times, this reliance on Chen's disclosure does not preclude the interpretation of being idle." Ans. 6.

Appellant's argument is unpersuasive of reversible Examiner error. Appellant fails to provide sufficient evidence of a meaning of "idle" that would exclude performing all processes rather than one or more of the recited storage device management activities, e.g., garbage collection. For example, Appellant fails to identify, and we are unable find, any description in the Specification of what constitutes a processor idle state. *See, e.g.*, Spec. ¶ 82. In the absence of sufficient evidence or reasoning and under a broad but reasonable interpretation, the disputed idle limitation is taught or suggested by Chen whereby switching of garbage collection from the DSDs

to the host controller places the DSDs in an idle state because the host controller assumes control of garbage collection rather than the DSD performing garbage collection.

Propriety of Combination

The Examiner concludes "[i]t would have been obvious . . . to incorporate Dillow's global garbage collection algorithm into Chen's garbage collection devices, as the optimization of garbage collection across multiple devices leads to 'minimize the degraded performance time and increase the optimal performance time of the entire array of devices.'" Final Act. 7 (citing Dillow, Abstract). Appellant contends "the only basis for the modification [of Chen to include the teachings of Dillow as] proposed by the Office appears to the features of the claims, which Appellant[] submit[s] would be inappropriate hindsight analysis." App. Br. 12. The Examiner responds

> [I]t must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper.

Ans. 5–6 (citing *In re McLaughlin*, 443 F.2d 1392 (CCPA 1971).

We agree with the Examiner. In contrast to Appellant's contention, we find the Examiner has articulated reasoning with rational underpinnings sufficient to justify the legal conclusion of obviousness. Final Act. 5; Ans. 5–6.

For the reasons discussed above, Appellant's arguments in connection with the rejection of claim 1 are unpersuasive of reversible Examiner error.

Accordingly, we sustain the rejection of independent claim 1 and, for the same reasons, the rejection of independent claims 8 and 15 under 35 U.S.C. § 103 as being unpatentable over Chen and Dillow. Furthermore, we sustain the rejections of dependent claims 2–7, 9–14, and 16–20 that are not argued separately with particularity.

DECISION

We affirm the Examiner's rejections under 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

Claims Rejected	**Basis**	**Affirmed**	**Reversed**
1–3, 8–10, 15–17	35 U.S.C. § 103 Chen, Dillow	1–3, 8–10, 15–17	
4, 7, 11, 14, 18	35 U.S.C. § 103 Chen, Dillow, Batwara	4, 7, 11, 14, 18	
5, 12, 19	35 U.S.C. § 103 Chen, Dillow, Batwara, Goss	5, 12, 19	
6, 13, 20	35 U.S.C. § 103 Chen, Dillow, Batwara, Shaharabany	6, 13, 20	
Overall Outcome		1–20	

AFFIRMED