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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DOE HYUN YOON, ROBERT SCHREIBER, and SHENG LI

Appeal 2018-007010
Application 14/648,290
Technology Center 2100

Before MICHAEL J. STRAUSS, IRVIN E. BRANCH, AND PHILLIP A. BENNETT, *Administrative Patent Judges.*

STRAUSS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Pursuant to 35 U.S.C. § 134(a), Appellant[1] appeals from the Examiner's decision to reject claims 1–4 and 6–19. Final Act. 2; Ans. 6. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse and enter a new ground of rejection pursuant to 37 C.F.R. § 41.50(b).[2]

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[1] We use the word "Appellant" to refer to "Applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies the real party in interest as Hewlett Packard Enterprise Development LP. Appeal Br. 1.

[2] We refer to the Specification, filed May 29, 2015 ("Spec."); Final Office Action, mailed August 23, 2017 ("Final Act."); Appeal Brief, filed January

CLAIMED SUBJECT MATTER

The claims are directed to memory controllers to form symbols based on bursts. Spec., Title. Claim 1, reproduced below with a disputed limitation emphasized in *italics*, is illustrative of the claimed subject matter:

> 1. A system comprising:
>
> a memory comprising a plurality of pins; and
>
> a memory controller to interface with the memory based on a codeword including a plurality of n-bit symbols, wherein *an n-bit symbol of the codeword is formed from a burst of a plurality of bits over time output by a single pin* of the plurality of pins of the memory,
>
> the memory controller to correct an error of the memory using the n-bit symbol formed from the burst of the plurality of bits.

REFERENCES[3]

The prior art relied upon by the Examiner is:

Dujari et al.	US 5,537,421	July 16, 1996
Deguchi et al.	US 2008/0126905 Al	May 29, 2008

The additional prior art relied upon in the new ground of rejection is:

Machado et al.	US 2004/0153902 A1	Aug. 5, 2004

REJECTION[4]

Claims 1–4 and 6–19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Deguchi and Dujari. Final Act. 6–10.

19, 2018 ("App. Br."); Examiner's Answer, mailed April 27, 2018 ("Ans."); and Reply Brief, filed June 27, 2018 ("Reply Br.").

[3] All citations herein to these references are by reference to the first named inventor only.

[4] The rejections of claims 1–19 under 35 U.S.C. § 112 and the rejection of claim 5 under 35 U.S.C. § 103 are withdrawn. Ans. 2, 6.

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellant's arguments that the Examiner has erred in rejecting independent claims 1, 10, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Deguchi and Dujari. We agree with Appellant's arguments as to this rejection of the claims.

The Examiner finds Deguchi discloses all the limitations of claim 1 except that it does not explicitly teach (i) a plurality of pins, wherein the n-bit symbol is formed from a burst of a plurality of bits over time output by one of the plurality of pins (the "single pin" limitation), and (ii) correcting an error using an 8-bit data (the "ECC" limitation"). Final Act. 7. The Examiner finds the ECC limitation is taught by Dujari. *Id.* In connection with the single pin limitation, the Examiner explains:

> Due to the fact that each of Deguchi's 8-bit memory chips (1004) provides a 8-bit of data and a 1-bit ECC, Deguchi shows that transfer lines (of 64 bits of data and 8 bits of ECC) are located between the chip set (1002) and the memory module (1001) (figure 1, ¶ [0007]). It would have been obvious to one skilled in the art before the effective filing date of the claimed invention to realize Deguchi's transfer lines (of 64 bits and 8 bits) would have been named as "plurality of pins" so that <u>each of the pins</u> transfers 8-bit of data and 1-bit of ECC between a corresponding Deguchi's memory chip (1004) and Deguchi's chip set (1002).

Id.

Appellant contends "[t]he Examiner has not explained how Deguchi provides any teaching or hint of forming an n-bit symbol of the codeword **from a burst of a plurality of bits output by a <u>single</u> pin** of a memory."

Appeal Br. 13. The Examiner responds, explaining, "there is no specific limit on the number of bits on 'a burst' nor 'a plurality of bits'. Therefore, each n-bit symbol can have any number of bits." Ans. 3. Thus, according to the Examiner, "each/one of Deguchi's transfer lines (1005) would have been named as a 'pin', so that each of the pins transfers an 8-bit of data." *Id.*at 4.

Appellant replies, arguing, contrary to the Examiner's interpretation, there is a lower limit on the number of bits in a burst, claim 1 reciting "a burst of a plurality of bits". Reply Br. 3. Appellant further argues, rather than a single pin or line, "[t]he transfer line 1005 from each memory chip 1004 as shown in Fig. 1 of Deguchi is 8 bits wide, and thus is connected to corresponding 8 pins of the memory chip 1004." *Id.*

Appellant's argument is persuasive of reversible error. Although Deguchi uses the singular noun form in describing bit line 1005 (Deguchi ¶ 7), inferring it is a single line, a close inspection of Figure 1 (depicted below) belies such a reading of the disclosure.

FIG. 1

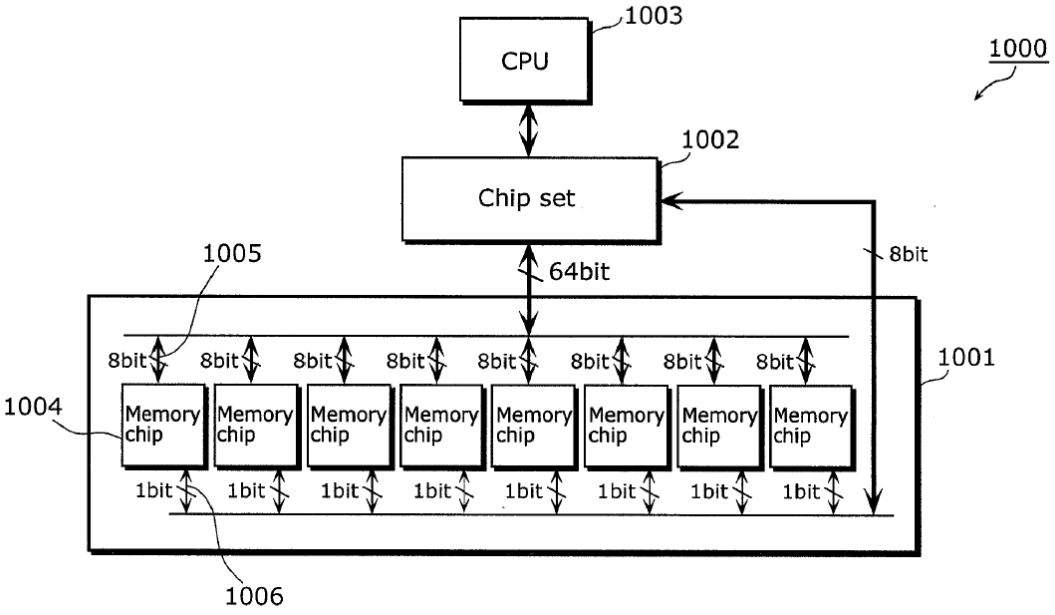

Figure 1 is a diagram showing a configuration of a conventional computer system.

In Figure 1 each bit line 1005 is represented by a single line with an arrow at each end and a slash or solidus (i.e., a "\" mark) through the line with the numeral "8" adjacent. One skilled in the art would have understood the slash mark with the numeral "8" adjacent means, rather than a single bit line, the single line depicted represents eight bit lines. This interpretation of the depicted schematic diagram or block drawing is consistent with graphic symbols standard use in electrical diagram as, for example, set forth in *Graphic Symbols for Electrical and Electronics Diagrams: (Including Reference Designation Class Designation Letters).* Institute of Electrical and Electronics Engineers, § 3.1.2.3 "'n' conductors or conductive paths," (1975) depicted below.

3.1.2.3 "n" conductors or conductive paths

NOTE — 3.1.2.3A: The "n" is not part of the symbol. A number representing the actual number of paths shall be substituted for "n".

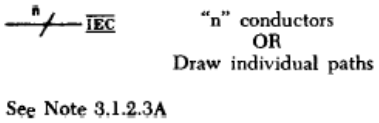

Figure 2: Graphic Symbol for "n" conductors or conductive paths

Accordingly, rather than disclosing a single line and, therefore, a single pin, Deguchi discloses an 8-bit wide bus having eight separate lines and, thereby, connected to eight pins, not a single pin. Furthermore, we agree with Appellant that it is improper to construe the recited symbols as each having a single bit in view of the argued claim language reciting an n-bit symbol of the codeword is formed from a burst of a *plurality* of bits over time output by a single pin. Therefore, it was reversible error for the Examiner to rely on Deguchi's bit lines for teaching the disputed single pin limitation. Because we agree with at least one of the arguments advanced by Appellant, we need not reach the merits of Appellant's other arguments.

For the reasons discussed above, we do not sustain the rejection of independent claim 1 or, for the same reasons, the rejection of independent claims 10 and 15 or the rejection of dependent claims 2–4, 6–9, 11–14, and 16–19 which stand with their respective base claim.

NEW GROUNDS OF REJECTION
35 U.S.C. § 102(b) and 35 U.S.C. § 103(a)

Pursuant to our authority under 37 C.F.R. § 41.50(b), we reject independent claims 1, 10, and 15 under 35 U.S.C. § 103(a) as being obvious

over Deguchi and Dujari further in view of Machado. The combination of Deguchi and Dujari teaches or suggests the limitations of claims 1, 10, and 15 as set forth in the Final Action at pages 6–8 except for the requirement of an n-bit symbol of the codeword formed from a burst of a plurality of bits over time output by a single pin of the plurality of pins of the memory.

Machado discloses a memory (serial flash memory 100) comprising a plurality of pins (Machado ¶ 63 – "A popular bit-Serial interface Specification is the Serial Peripheral Interface ("SPI") protocol, which uses the four signal pins Data In, Data Out, Clock and Chip Select."); a memory controller (ECC 140 performing one-bit corrections and external software, firmware or hardware performing two-bit corrections) to interface with the memory based on a codeword including a plurality of n-bit symbols, wherein an n-bit symbol of the codeword is formed from a burst of a plurality of bits over time (Machado ¶ 104: "For each byte of the user data 210 in the shift register 130, the bits are serially shifted out and furnished to the I/O interface 190 via the demultiplexer 142 and the multiplexer 144.") output by a single pin (Machado ¶ 63 – Data Out signal pin) of the plurality of pins of the memory (Machado ¶ 63: SPI uses four signal pins). Machado further discloses the memory controller corrects memory errors using the n-bit symbol formed from the burst of the plurality of bits (Machado ¶ 62: "One bit corrections are done automatically in hardware during reads or transfer to the page memory 120 (AutoCorrect), while two-bit corrections are handled in external Software, firmware or hardware" (i.e., on or from the serialized data.); *see also* Machado ¶ 20: "serial ECC systems use less chip area.")

It would have been obvious to one skilled in the art at the time the

invention was made to use Machado's serial output in the Deguchi's chip set to reduce a pin count and for compatibility with serial devices, e.g., serial data buses.

Remaining claims

Although we have rejected the independent claims under 37 C.F.R. § 41.50(b), we have not reviewed the remaining claims to the extent necessary to determine whether these claims are unpatentable under 35 U.S.C. §§ 102 or 103. We leave it to the Examiner to determine the appropriateness of any further rejections based thereon.

DECISION

We reverse the Examiner's decision to reject claims 1–4 and 6–19 under 35 U.S.C. § 103(a).

Pursuant to our discretionary authority under 37 C.F.R. § 41.50(b), we newly reject claims 1, 10, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Deguchi, Dujari, and Machado.

Rule 37 C.F.R. § 41.50(b) provides "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review." 37 C.F.R. § 41.50(b) also provides:

When the Board enters such a non-final decision, Appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground[s] of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter

> reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground[s] of rejection [are] binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground[s] of rejection designated in [this] decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to a new ground of rejection can be found in the Manual of Patent Examining Procedure § 1214.01.

REVERSED
37 C.F.R. § 41.50(b)