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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte TOBIAS SCHEUER

Appeal 2018-006364
Application 14/657,421
Technology Center 2100

Before JOSEPH L. DIXON, JAMES W. DEJMEK, and STEPHEN E. BELISLE, *Administrative Patent Judges*.

BELISLE, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant[1] appeals under 35 U.S.C. § 134(a) from a final rejection of all pending claims, namely, claims 1–20. App. Br. 4. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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[1] Appellant identifies SAP SE (Germany) as the real party in interest. App. Br. 2.

STATEMENT OF THE CASE

The Claimed Invention

Appellant's invention generally relates to a sampling-based central processing unit ("CPU") profiler that determines a CPU time usage for at least one activity of a plurality of activities serviced by a CPU in order to identify times when the CPU is idle. Spec. ¶ 2.

An exemplary embodiment of such a CPU profiler is described in Appellant's Specification using Figure 3, reproduced below.

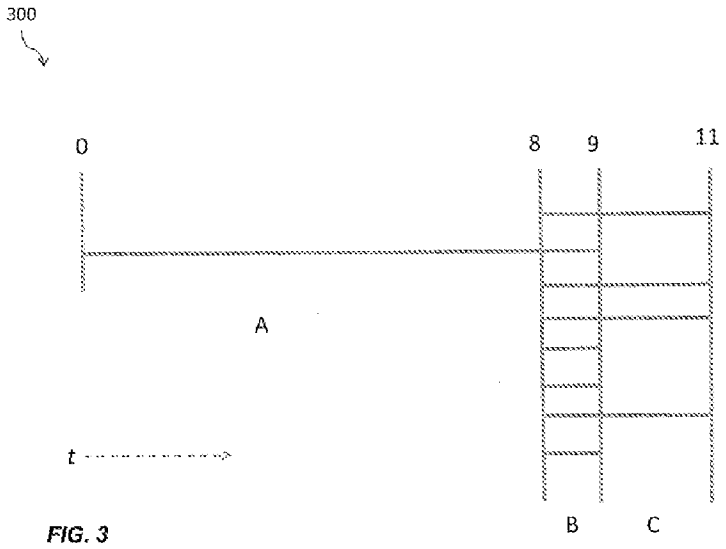

FIG. 3

Figure 3 is a diagram illustrating one example of determining a CPU time usage for at least one activity of a plurality of activities serviced by a CPU. Spec. ¶ 15. According to Appellant, Figure 3 "illustrates work that consists of 8 seconds serial execution (A) followed by another 8 seconds being executed in parallel (B) on 8 threads, followed by yet another 8 seconds of work (C) being executed on 4 threads." Spec. ¶ 24. More specifically, in Figure 3:

> [T]ime is on the X-axis, [and] 0[,] 8, 9, and 11 seconds are indicated. The rows are the threads, and the visible part is where the thread is busy. The target for the measurement in this

> example is 8 threads. Then, during the first 8 seconds, the samples see 1 busy thread A using all of the CPU, and 7 threads not doing work. So the samples CPU times (8 seconds each) would be multiplied by 7, accounting for 56 seconds of wasted CPU. Then in the ninth second, the samples will see 8 threads working B, but the difference is 0 so the CPU times will not be accounted. During the last two seconds, the samples see 4 busy threads and 4 idle threads, so the difference is 1 [sic: 4] and C will get 8 seconds of waste.

Spec. ¶ 25. According to Appellant, "[t]he classical profiling would tell us that A, B and C are getting 8 seconds of CPU each, or 33%, but that does not indicate how the total of 11 seconds of execution time is spent." Spec. ¶ 24. Rather, "[figure] 3 clearly shows that a developer should look mostly at the part A to improve, and then C. Part B is good as there is no waste because that part is already using all target threads." Spec. ¶ 26.

Claim 1, reproduced below with bracketed notations added, is illustrative of the claimed subject matter on appeal:

> 1. A method comprising:
>
> [(a)] identifying, by at least one processor of a computing system, an activity of a plurality of activities serviced by one or more central processing units (CPUs), each activity being performed by one or more computing threads of a plurality of computing threads executing a plurality of subroutines of a computer program;
>
> [(b)] counting, by the at least one processor, a number of active computing threads that are performing the activity for each of a plurality of separate time periods to generate a count of a plurality of counts for each of the plurality of separate time periods, a sum of time for which each active computing thread performs the activity during each separate time period being same for each separate time period;
>
> [(c)] setting, by the at least one processor, a target representing a highest count among the plurality of counts;

> [(d)] determining, by the at least one processor, a number of active computing threads that are performing the activity within a particular time period of the plurality of separate time periods by using the one or more CPUs;
>
> [(e)] calculating, by the at least one processor, a number of inactive computing threads that are not performing the activity within the particular time period and not using the one or more CPUs by computing a difference between the target and the number of active threads;
>
> [(f)] generating, by the at least one processor, a central processing unit time usage for the activity by multiplying a time duration of the activity by a value obtained by dividing the number of inactive threads by the number of active threads; and
>
> [(g)] providing, by the at least one processor, data comprising the central processing unit time usage.

Rejections

The Examiner made the following rejections of the claims on appeal:[2]

Claims 1, 7, and 14 stand rejected under 35 U.S.C. § 101 for being directed to patent-ineligible subject matter. Final Act. 9.

Claims 1–20 stand rejected under 35 U.S.C. § 112(a) for failing to comply with the written description requirement. Final Act. 3.

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[2] The Examiner also had rejected all of the claims on appeal under (1) 35 U.S.C. § 112(a) for failing to comply with the enablement requirement (Final Act. 6), and (2) 35 U.S.C. § 103 (Non-Final Rejection, mailed Dec. 30, 2016, pp. 6–13; Final Act. 9). However, the Examiner subsequently withdrew those rejections: "Appellant has provided four main arguments (A-D) in the appeal brief. The arguments in A [enablement] refer to a previously withdrawn enablement rejection, and the arguments in D [obviousness] refer to the previously withdrawn prior art rejections. The Office considers those points moot and will address arguments B [written description] and C [§ 101] . . . ." Ans. 10.

ANALYSIS[3]

Subject Matter Eligibility

We review the Examiner's Section 101 rejection of independent claims 1, 7, and 14 in light of Appellant's arguments that the Examiner erred. We find Appellant's Section 101 arguments unpersuasive.

Section 101 provides that a patent may be obtained for "any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof." 35 U.S.C. § 101. However, Section 101 includes implicit exceptions: "[l]aws of nature, natural phenomena, and abstract ideas" are not patentable. *Alice Corp. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014). Key concepts identified by the courts as abstract ideas include concepts in the following three groupings: mathematical concepts;[4] certain methods of organizing human activity;[5] including fundamental economic principles or practices; and mental processes, including

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[3] Throughout this Decision, we have considered Appellant's Appeal Brief filed January 8, 2018 ("App. Br."); Appellant's Reply Brief filed June 4, 2018 ("Reply Br."); the Examiner's Answer mailed April 4, 2018 ("Ans."); the Final Office Action mailed June 6, 2017 ("Final Act."); and Appellant's Specification filed March 13, 2015 ("Spec.").

[4] *See, e.g.*, *Gottschalk v. Benson*, 409 U.S. 63, 71–72 (1972); *Bilski v. Kappos*, 561 U.S. 593, 611 (2010); *Mackay Radio & Telegraph Co. v. Radio Corp. of Am.*, 306 U.S. 86, 94 (1939); *SAP America v. InvestPic*, 898 F.3d 1161, 1163 (Fed. Cir. 2018).

[5] *See, e.g.*, *Bilski*, 561 U.S. at 611–612; *Alice*, 573 U.S. at 219–20; *Ultramercial v. Hulu*, 772 F.3d 709, 715 (Fed Cir. 2014).

observations, evaluations, judgments, or opinions.[6] *See* 2019 Guidance at 52 n.12–15. To determine whether a claim falls within these exceptions, we are guided by the Supreme Court's two-step framework described in *Alice* (implemented as Steps 2A and 2B in the 2019 Guidance[7]). *Id.* at 217–18 (citing *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 75–77 (2012)).

STEP 1

Claim 1, as a method claim, recites one of the enumerated categories of statutory subject matter in 35 U.S.C. § 101, namely, a process. The issue before us is whether it is directed to a judicial exception without significantly more.

STEP 2

The Supreme Court's two-step framework requires:

> First, . . . determine whether the claims at issue are directed to one of those patent-ineligible concepts. If so, we then ask, "[w]hat else is there in the claims before us?" To answer that question, . . . consider the elements of each claim both individually and "as an ordered combination" to determine whether the additional elements "transform the nature of the claim" into a patent-eligible application. [The Court] described step two of this analysis as a search for an "'inventive concept'"—i.e., an element or combination of elements that is "sufficient to ensure that the patent in practice amounts to

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[6] *See, e.g.*, *Benson*, 409 U.S. at 67; *CyberSource Corp. v. Retail Decisions*, 654 F.3d 1366, 1371–72 (Fed. Cir. 2011); *Intellectual Ventures I v. Symantec Corp.*, 838 F.3d 1307, 1318 (Fed. Cir. 2016).

[7] For continuity of analysis, we adopt the "steps" nomenclature from the USPTO's 2019 Revised Patent Subject Matter Eligibility Guidance, 84 Fed. Reg. 50 (Jan. 7, 2019) ("2019 Guidance").

> significantly more than a patent upon the [ineligible concept] itself."

Alice, 573 U.S. at 217–18 (citations omitted). To perform this test, we must first determine whether the claim is "directed to" one of the judicially recognized exceptions, namely, laws of nature, natural phenomena, or abstract ideas. *Alice*, 573 U.S. at 217. As part of this inquiry, we must "look at the 'focus of the claimed advance over the prior art' to determine if the claim's 'character as a whole' is directed to excluded subject matter." *Affinity Labs of Tex., LLC v. DirecTV, LLC*, 838 F.3d 1253, 1257–58 (Fed. Cir. 2016) (internal citations omitted). Per the 2019 Guidance, this first inquiry has two prongs of analysis: (i) does the claim recite any judicial exceptions (Step 2A, Prong 1), and (ii) if so, is the judicial exception integrated into a practical application (Step 2A, Prong 2). *See* 2019 Guidance at 54. Finally, if the claim is directed to a judicial exception, then we determine whether the claim provides an inventive concept because any additional elements recited in the claim provide significantly more than the recited judicial exception (Step 2B).

STEP 2A, Prong 1

Method claim 1 recites, in part: "*counting* . . . *a number* of active computing threads . . ." (step (b)); "*setting* . . . *a target* representing a highest count among the plurality of counts" (step (c)); "*determining* . . . *a number* of active computing threads . . ." (step (d)); "*calculating* . . . *a number* of inactive computing threads . . . *by computing a difference*" (step (e)); and "*generating* . . . *a central processing unit time usage* for the activity *by multiplying* a time duration of the activity *by a value* obtained *by dividing the number* of inactive threads *by the number* of active threads . . ." (step (f)) (emphases added). These steps of counting, determining, calculating, and

generating (steps (b), (d), (e), and (f), respectively) perform calculations using basic math, namely, addition, subtraction, multiplication, and division. Likewise, the step of setting a target (step (c)) establishes a numerical threshold relationship for purposes of calculating active versus inactive threads. Accordingly, we conclude claim 1 recites mathematical calculations and relationships, which are mathematical concepts identified in the 2019 Guidance, and thus an abstract idea. *See SAP Am.*, 898 F.3d at 1163, 1167 (holding claims to a "series of mathematical calculations based on selected information" are directed to abstract ideas). Therefore, we proceed to Step 2A, Prong 2.

STEP 2A, Prong 2

The next issue is whether the recited judicial exception is integrated into a practical application of that exception.[8]

> At the same time, we tread carefully in construing this exclusionary principle lest it swallow all of patent law. At some level, "all inventions . . . embody, use, reflect, rest upon, or apply laws of nature, natural phenomena, or abstract ideas." Thus, an invention is not rendered ineligible for patent simply because it involves an abstract concept. "[A]pplication[s]" of such concepts "'to a new and useful end,'" we have said, remain eligible for patent protection. Accordingly, in applying the § 101 exception, we must distinguish between patents that claim the "'buildin[g] block[s]'" of human ingenuity and those that integrate the building blocks into something more, thereby "transform[ing]" them into a patent-eligible invention.

Alice, 573 U.S. at 217 (citations omitted).

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[8] *See, e.g.*, *Alice*, 573 U.S. at 223, discussing *Diamond v. Diehr*, 450 U.S. 175 (1981).

The introduction of a computer into the claims does not alter the analysis at *Alice* step two (implemented in part as Step 2A, Prong 2 in the 2019 Guidance).

> [T]he mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention. Stating an abstract idea "while adding the words 'apply it'" is not enough for patent eligibility. Nor is limiting the use of an abstract idea "'to a particular technological environment.'" Stating an abstract idea while adding the words "apply it with a computer" simply combines those two steps, with the same deficient result. Thus, if a patent's recitation of a computer amounts to a mere instruction to "implement[t]" an abstract idea "on . . . a computer," that addition cannot impart patent eligibility. This conclusion accords with the preemption concern that undergirds our § 101 jurisprudence. Given the ubiquity of computers, wholly generic computer implementation is not generally the sort of "additional featur[e]" that provides any "practical assurance that the process is more than a drafting effort designed to monopolize the [abstract idea] itself."

Alice, 573 U.S. at 223–224 (citations omitted). "[T]he relevant question is whether the claims here do more than simply instruct the practitioner to implement the abstract idea . . . on a generic computer." *Alice*, 573 U.S. at 225. To answer this question, we ask whether claim 1 as a whole integrates the recited judicial exception (here, mathematical concepts) into a practical application of the exception. *See* 2019 Guidance at 54.

In short, claim 1 calculates CPU time usage data (App. Br. 18 ("focus of pending claim 1 is on computing CPU time usage")), but claim 1 itself does nothing practically to apply that data. Contrary to Appellant's contentions (*see* App. Br. 16–19; Reply Br. 14–18), we find claim 1 does not improve the functioning of a computer or improve another technology or technical field. Again, as drafted, claim 1 does not change the functioning

of a computer in any way, and Appellant has not evidenced any such change, let alone an improvement in computer functionality. In addition, the remaining steps of (a) identifying CPU-serviced activities being performed by threads and (g) providing data add insignificant extra-solution activity to the recited mathematical relationships and calculations. *See Parker v. Flook*, 437 U.S. 584, 588–90 (1978) (holding that a step of adjusting an alarm limit variable to a figure computed according to a mathematical formula was "post-solution activity"); *see also Electric Power Group, LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016) (claims focused on "collecting information, analyzing it, and displaying certain results of the collection and analysis" are directed to an abstract idea); MPEP § 2106.05(g). Accordingly, we agree with the Examiner[9] and conclude claim 1 does not integrate the judicial exception into a practical application, i.e., claim 1 is directed to an abstract idea.

STEP 2B

The next issue is whether claim 1 provides an inventive concept because additional elements recited therein provide significantly more than the recited judicial exception. Taking the claim elements separately, the function performed by the computer at each step of the process is purely conventional. Using a computer processor for identifying, counting, setting, determining, calculating, generating, and providing data (i.e., steps (a)–(g)) amounts to electronic data query, retrieval, and analysis—some of the most

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[9] Ans. 12 (Examiner finding "the limitations of the claims reasonably correspond to the mere collecting, analyzing, and displaying of information that the Courts have interpreted as an abstract idea . . . ."); Final Act. 9.

basic functions of a computer. All of these computer functions in steps (a) through (g), as presently drafted, are generic, routine, and conventional computer activities that are performed only for their conventional uses. *See Elec. Power Grp.*, 830 F.3d at 1355. None of these activities are used in some unconventional manner nor do any produce some unexpected result, and Appellant does not contend to have invented any of these activities. Moreover, as presently drafted, the method of claim 1 produces CPU time usage data *without any practical application thereof.* In short, each step does no more than require a generic computer to perform generic computer functions. *Cf.* Spec., Claim 6. As to the data operated upon, "even if a process of collecting and analyzing information is 'limited to particular content' or a particular 'source,' that limitation does not make the collection and analysis other than abstract." *SAP Am.*, 898 F.3d at 1168.

Considered as an ordered combination, the steps of Appellant's method claim 1 add nothing that is not already present when the steps are considered separately. The sequence of data identification–reception–analysis–modification–presentation is equally generic and conventional or otherwise held to be abstract. *See* Ans. 13 ("There is no indication that the combination of the elements improves the functioning of a computer or improves any other technology, they merely use existing technology for the same purpose for which it was intended."); *see also Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 714–16 (Fed. Cir. 2014) (sequence of receiving, selecting, offering for exchange, displaying, allowing access, and receiving payment recited an abstraction); *Two-Way Media Ltd. v. Comcast Cable Communications, LLC*, 874 F.3d 1329, 1339 (Fed. Cir. 2017) (sequence of processing, routing, controlling, and monitoring data recited an abstraction).

Therefore, we find the ordering of the steps in claim 1 is ordinary and conventional.

We again agree with the Examiner,[10] and conclude claim 1 does not provide an inventive concept because the additional elements recited in the claim do not provide significantly more than the recited judicial exception. *See* Final Act. 9. Accordingly, we sustain the Examiner's rejection of independent claim 1 as being patent ineligible under 35 U.S.C. § 101. For similar reasons, we also sustain the Examiner's rejection under 35 U.S.C. § 101 of independent claims 7 and 14, which recite commensurate limitations as claim 1 and for which Appellant relies on the same arguments as those advanced with respect to claim 1.[11]

Written Description

The Examiner rejected claims 1, 7, and 14, and all corresponding dependent claims, namely, claims 2–6, 8–13, and 15–20, under 35 U.S.C. § 112(a) for failing to comply with the written description requirement. *See* Final Act. 3. Specifically, the Examiner finds Appellant's Specification lacks written description for the following three claim limitations:

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[10] Ans. 13 (Examiner finding independent claims recite "generic computer components performing generic computer functions that are well-understood, routine and conventional activities previously known to the industry that do not amount to significantly more than the judicial exception.").

[11] The Examiner expressly rejected only the independent claims, namely, claims 1, 7, and 14, under 35 U.S.C. § 101, although the Examiner did briefly comment on patent eligibility concerning dependent claims 6, 13, and 20. Final Act. 9. As such, our Decision in this regard is limited to the independent claims.

> (1) "identifying . . . an activity of a plurality of activities *serviced by one or more central processing units (CPUs)*" ("Identifying Limitation"), Final Act. 4; *see* claims 1, 7, 14;
>
> (2) "counting, by the at least one processor, a number of active computing threads that are performing the activity for each of a plurality of separate time periods to generate a count of a plurality of counts for each of the plurality of separate time periods, a sum of time for which each active computing thread performs the activity during each separate time period being same for each separate time period" ("Counting Limitation"), Final Act. 4; *see* claims 1, 7, 14; and
>
> (3) "wherein the CPU usage time is used to modify the execution of the computer program such that the modified computer program is more efficient than the computer program before the modification" ("Modifying Limitation"), Final Act. 5–6; *see* claims 6, 13, 20.

The purpose of the written description requirement is to "'ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification.'" *Univ. of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 920 (Fed. Cir. 2004) (quoting *Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000)). This requirement protects the *quid pro quo* between inventors and the public, whereby the public receives "meaningful disclosure in exchange for being excluded from practicing the invention for a limited period of time." *Enzo Biochem, Inc. v. Gen–Probe Inc.*, 323 F.3d 956, 970 (Fed. Cir. 2002). To satisfy the written description requirement, the disclosure must reasonably convey to skilled artisans that Appellant possessed the claimed invention as of the filing date. *See Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). "The invention is, for purposes of the 'written description' inquiry, *whatever is now claimed*." *Vas–Cath Inc. v. Mahurkar*, 935 F.2d 1555,

1563–64 (Fed. Cir. 1991). Such description need not recite the claimed invention *in haec verba* but must do more than merely disclose that which would render the claimed invention obvious. *See Univ. of Rochester*, 358 F.3d at 923; *Regents of the Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1566–67 (Fed. Cir. 1997); *see also PowerOasis, Inc. v. T–Mobile USA, Inc.*, 522 F.3d 1299, 1306–07 (Fed. Cir. 2008) (explaining that § 112(a) "requires that the written description actually or inherently disclose the claim element").

Identifying Limitation

As for the Identifying Limitation, Appellant argues "the use of multiple CPUs to service activities that are performed by threads is fully supported by the patent application, at least at paragraphs [0004], [0006], [0008], and [0037]." App. Br. 14; Reply Br. 7–8. The Examiner finds (1) "Appellant has impermissibly amended the claims to include monitoring threads running on multiple CPUs rather than a single CPU as detailed throughout the Specification" (Ans. 5); (2) many instances in the Specification where Appellant describes the invention in terms of "a" (singular) CPU (*see* Ans. 5–7); and (3) the difference between monitoring threads running on multiple versus a single CPU "is not a semantic triviality" (Ans. 7).

The Identifying Limitation recites, in part, "identifying . . . an activity of a plurality of activities serviced by one or more central processing units (CPUs)," which we construe broadly, but reasonably, to mean selecting (for subsequent evaluation) one activity out of a plurality of CPU-serviced

activities.[12] Although Appellant's cited Specification paragraph 37 does not exist, we do find written description support in the Specification for the Identifying Limitation as construed above at Appellant's other citations. *See* Spec. ¶ 4 ("[a] CPU profiler is described that can collect data about *usage of central processing units (CPUs) [plural] by various activities or threads*"); Spec. ¶ 6 ("CPU can be one of *a plurality of CPUs*"); Spec. ¶ 8 ("CPU can be one of *a plurality of CPUs*, the plurality of CPUs being optimally used when the number of busy threads is equal to the target.") (Emphases added.) We find the Examiner's arguments here concerning "threads" running on multiple CPUs appropriately directed to the Counting Limitation discussed below.

Accordingly, we do not sustain the Examiner's rejection of claims 1–20 under 35 U.S.C. § 112(a) as to the Identifying Limitation.

Counting Limitation

Appellant's written description arguments in the Appeal Brief concern only the Identifying Limitation and Modifying Limitation. Appellant belatedly proffered written description arguments concerning the Counting Limitation in the Reply Brief. These Counting Limitation arguments could have been made in the Appeal Brief, and are not responsive to any new

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[12] We do not opine herein on whether Appellant's Identifying Limitation complies with 35 U.S.C. § 112(b) (definiteness), and leave it to the Examiner to further consider this issue in any further prosecution on the merits (e.g., whether "serviced by" modifies "an activity" or rather "a plurality of activities," and if the latter, still whether any one activity is "serviced by" multiple CPUs). Although the Board is authorized to reject claims under 37 C.F.R. § 41.50(b), no inference should be drawn when the Board elects not to do so. *See* MPEP § 1213.02.

evidence or finding set forth by the Examiner in the Answer. In the absence of a showing of good cause by Appellant, these arguments are untimely and deemed waived.

> Any argument raised in the reply brief which was not raised in the appeal brief, or is not responsive to an argument raised in the [E]xaminer's answer, including any designated new ground of rejection, will not be considered by the Board for purposes of the present appeal, unless good cause is shown.

37 C.F.R. § 41.41(b)(2) (2017); *see also Ex parte Nakashima*, 93 USPQ2d 1834, 1837 (BPAI 2010) (informative) (explaining that arguments and evidence not presented timely in the principal brief will not be considered when filed in a reply brief, absent a showing of good cause explaining why the argument could not have been presented in the principal brief); *Ex parte Borden*, 93 USPQ2d 1473, 1474 (BPAI 2010) (informative) ("[T]he reply brief [is not] an opportunity to make arguments that could have been made in the principal brief on appeal to rebut the Examiner's rejections, but were not.").

Notwithstanding the tardiness of such arguments, we do not find Appellant's Counting Limitation written description arguments persuasive. Appellant argues "[w]hile the [Counting Limitation] . . . recites multiple threads, nowhere does this feature require execution of those threads in parallel *on a single processor*, as alleged by the Examiner," and this limitation "does not anywhere recite multiple threads being executed in parallel *on a single processor* . . . ." Reply Br. 8–9. The Examiner finds, based on Appellant's own remarks during prosecution concerning Figure 3, the Counting Limitation includes within its scope counting multiple threads running in parallel on a single processor, but finds no written description reasonably to convey *Appellant* possessed how to do so at the time of filing.

See Final Act. 4–5; Reply Br. 7–9. Here, we agree with the Examiner that the Specification lacks written description for the *full scope* of the Counting Limitation. *See Atlantic Research Marketing Sys., Inc. v. Troy*, 659 F.3d 1345, 1355 (Fed. Cir. 2011) (holding invalid claims that exceeded in scope the subject matter that inventor chose to disclose to the public in the written description).

Although Appellant argues the Counting Limitation does not "require" counting multiple threads running in parallel on a single processor, Appellant nevertheless has argued that doing so is *within the scope* of the Counting Limitation as presently drafted. *See* Reply Br. 8–9. Indeed, Appellant argued Figure 3 shows eight threads executed in parallel by one CPU, and is "consistent" with the Counting Limitation. *See* Appellant's Reply to Non-Final Office Action of Dec. 30, 2016, filed Mar. 28, 2017, at 8–11 (arguing Figure 3 is "consistent" with the Counting Limitation); Reply Br. 9 ("claim 1 was amended previously during prosecution to recite features supported by the patent application at, among other places, FIG. 3"); Spec. ¶ 15 (describing Figure 3 as showing "activities serviced by a [CPU]" (emphasis added)); Spec. ¶¶ 24–25 (discussing Figure 3 as showing "8 threads" running "in parallel" on "the CPU"). Yet the Examiner finds that "figure [3], and the entire Specification for that matter, fails to appreciate the difference between parallel and sequential execution, parallel requiring multiple processors," and "[b]ecause threads cannot run in parallel on a single processor, as claimed by Applicant," Appellant "did not possess the claimed invention at the time of filing . . . ." Final Act. 5. In other words, the Examiner finds that, because the present scope of the Counting Limitation includes counting multiple threads running in parallel on one

CPU, and because Appellant's Specification lacks disclosure showing *Appellant* possessed how to accomplish such counting, the Counting Limitation lacks written description.

Appellant responds "the Examiner has failed to contemplate that one of ordinary skill in the art would readily understand the concepts of multiple logical cores running on a single CPU," and asserts that a cited Wikipedia page "clarifies that a single CPU can have multiple processing units, which can be referred to as cores, and that multiple threads can run concurrently on a single CPU." Reply Br. 10. In earlier prosecution, the Examiner had addressed this argument:

> Upon apparently now grasping that a single CPU cannot, in fact, run more than one thread at any given time, however, Applicant now argues, and without Specification support, that the single CPU referenced throughout the disclosure is really a "multicore" processor. A "processor," a "CPU," and a "core," are all synonymous in the art. Multi-core is the same as multi-processor. Just as one skilled in the art would not interpret the term "a CPU" to mean "multiple CPUs," one would not also interpret the term "a CPU" to mean "multicore processor." Applicant's argument, while unpersuasive and unsupported in the Specification, does inadvertently bolster the Examiner's rejections. As stated previously, managing multi-threading on a single processor and managing parallel threads across multiple processors are fundamentally different problems, neither of which are clearly addressed in the Specification.

Advisory Action Before the Filing of an Appeal Brief, mailed Aug. 29, 2017, at 2. Although Appellant cites to *outside* the Specification (i.e., a Wikipedia page) to show what *the skilled artisan* may understand concerning multiple logic cores, Appellant has not cited any support *inside* the Specification (i.e., written description) to show *Appellant possessed* the full scope of the Counting Limitation, which (as found by the Examiner and

argued by Appellant) encompasses multiple threads running in parallel on one CPU. For example, Appellant does not point to any disclosure in the Specification showing *Appellant* possessed running multiple threads in parallel using multiple logic cores, and more importantly, showing *Appellant* possessed how to count such threads running on multiple logic cores. We find Appellant's Counting Limitation written description arguments unpersuasive of Examiner error.

Accordingly, we sustain the Examiner's rejection of claims 1–20 under 35 U.S.C. § 112(a) as to the Counting Limitation.

Modifying Limitation

Appellant argues the Modifying Limitation "is fully supported by the patent application, at least at original claims 6, 13 and 20, as well as paragraphs [0006], [0008], [0010], and [0037]." App. Br. 15; Reply Br. 10–11. The Examiner finds the "Specification is devoid of any detail or examples demonstrating how such CPU usage time could be used to modify program code to be more efficient" (Final Act. 6), and "[j]ust as the CPU outlined in FIG. 3 cannot logically exist, much less be monitored, the Appellant could not have been in possession of a method for modifying code to make it run more efficiently on a processor that does not, and logically cannot, exist" (Ans. 9).

Here again, we agree with Appellant that the Specification provides adequate written description support for the Modifying Limitation. This limitation recites, in part, using the calculated CPU time usage to modify a computer program. Although we note again that Appellant's cited Specification paragraph 37 does not exist, we do find adequate written description support in the Specification for the Modifying Limitation at

Appellant's other citations. *See* Spec. ¶¶ 6, 8 ("The CPU time usage for the activity can be used (for example, by a developer) to modify execution of the computer program. The modified execution of the computer program can be more efficient than execution of the computer program before the modification."); Spec. ¶ 10 ("The computing device can execute an application that enables an analysis of the CPU usage time to modify execution of the computer program."). We find a skilled artisan would understand the Specification reasonably to convey Appellant possessed using CPU time usage to guide a developer to modify particular aspects of a computer program to improve the execution efficiency thereof. *See* Spec. ¶ 26 ("FIG. 3 clearly shows that a developer should look mostly at the part A to improve, and then C. Part B is good as there is no waste because that part is already using all target threads . . . ."). We also find the Examiner's arguments here concerning "a processor that does not . . . exist" appropriately directed to the Counting Limitation discussed above.

Accordingly, we do not sustain the Examiner's rejection of claims 6, 13, and 20 under 35 U.S.C. § 112(a) as to the Modifying Limitation.

DECISION

We affirm the Examiner's decision rejecting claims 1, 7, and 14 under 35 U.S.C. § 101.

We affirm the Examiner's decision rejecting claims 1–20 under 35 U.S.C. § 112(a) as to the Counting Limitation.

We reverse the Examiner's decision rejecting claims 1–20 under 35 U.S.C. § 112(a) as to the Identifying Limitation.

We reverse the Examiner's decision rejecting claims 6, 13, and 20 under 35 U.S.C. § 112(a) as to the Modifying Limitation.

Because we affirm at least one ground of rejection with respect to each claim on appeal, the Examiner's decision rejecting claims 1–20 is affirmed. *See* 37 C.F.R. § 41.50(a)(1).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

AFFIRMED