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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte THOMAS A. PHELAN, MICHAEL MORETTI, and DRAGAN STANCEVIC

Appeal 2018-006173
Application 14/330,947[1]
Technology Center 2100

BEFORE MICHAEL J. STRAUSS, JON M. JURGOVAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant seeks review under 35 U.S.C. § 134(a) from a Final Rejection of claims 1–17. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.[2]

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[1] We use the word "Appellant" to refer to "applicant(s)" as defined in 37 C.F.R. § 1.42. According to Appellant, the real party in interest is BLUEDATA SOFTWARE, INC. Appeal Br. 2.

[2] Our Decision refers to the Specification ("Spec.") filed July 14, 2014, the Final Office Action ("Final Act.") mailed July 20, 2017, the Appeal Brief ("Appeal Br.") filed February 2, 2018, the Examiner's Answer ("Ans.") mailed March 29, 2018, and the Reply Brief ("Reply Br.") filed May 29, 2018.

CLAIMED INVENTION

The claims are directed to accelerating data input and output in a virtual environment. Spec. ¶ 5. A translation node passes a process identifier to a kernel driver for a host environment. *Id.* ¶ 6. The process identifier identifies a guest element spawned in a virtual machine. *Id.* The kernel driver uses the process identifier to determine an allocation of host memory and its correspondence to an allocation of guest memory, and returns the allocation of host memory to the translation node. *Id.*

Claims 1 and 10 are independent. The remaining claims are dependent from one of these two claims. Claim 1, reproduced below with argued language emphasized, is representative of the claimed subject matter:

> 1. An apparatus comprising:
>
> one or more computer readable storage media;
>
> program instructions stored on the one or more computer readable storage media that, when executed by a processing system to facilitate accelerated input and output with respect to a virtual environment, direct the processing system to at least:
>
> pass a process identifier from a translation node to a kernel driver for a host environment, wherein the process identifier identifies a guest element spawned in a virtual machine and wherein the kernel driver uses the process identifier to determine an allocation of host memory corresponding to guest memory for the guest element, *store memory allocation information about the allocation of host memory in a data structure, and return a location of the memory allocation information in the data structure to the translation node*;
>
> in the translation node, perform a mapping of the allocation of host memory to an allocation of guest memory for the guest element using the location of the memory allocation information.

Appeal Br. 10 (Claims App.) (emphasis added).

REJECTIONS

Claims 1–3, 5, 6, 10–12, and 14 stand rejected under 35 U.S.C. § 103 as obvious over Tsirkin (US 2012/0072906 A1, published March 22, 2012) and Suzuki (US 2013/0047157 A1, published February 21, 2013). Final Act. 5–9.

Claims 4 and 13 stand rejected under 35 U.S.C. § 103 as obvious over Tsirkin, Suzuki, and Schug (US 2002/0091863 A1, published July 11, 2002). Final Act. 9–11.

Claims 7–9 and 15–17 stand rejected under 35 U.S.C. § 103 as obvious over Tsirkin, Suzuki, and Dong (US 2013/0055259 A1, published February 28, 2013). Final Act. 11–14.

ANALYSIS

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) where present, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Obviousness Rejection of Claims 1–3, 5, 6, 10–12, and 14

Appellant argues similar limitations of independent claims 1 and 10 together as one group and presents no separate arguments for the dependent claims. Appeal Br. 8. Accordingly, we select claim 1 as representative and address only this claim in our analysis. *See* 37 C.F.R. § 41.37(c)(1)(iv).

Claim 1 recites "the kernel driver uses the process identifier to determine an allocation of host memory corresponding to guest memory for the guest element, *store memory allocation information about the allocation of host memory in a data structure, and return a location of the memory allocation information in the data structure to the translation node*." Appeal Br. 10 (Claims App.) (emphasis added). Appellant argues Tsirkin fails to disclose this claim limitation, as follows:

> Tsirkin fails to disclose an element equivalent to the kernel driver of claim 1 that returns a location of memory allocation information to an element equivalent to the translation node of claim 1. In fact, Tsirkin fails to discuss the return, or otherwise passing, of a location of information of any kind much less memory allocation information. Rather, Tsirkin merely discloses that a bus address and offset are used to indicate where a DMA buffer starts and the size of the DMA buffer, respectively (see Tsirkin, ¶ 0036). Even if a bus address is considered a location, Tsirkin does not discuss what information is stored at that location and therefore does not disclose that the bus address is a location of memory allocation information, as required by claim 1. Likewise, even if the bus address and offset were themselves considered memory allocation information, Tsirkin never describes that the bus address and offset would be stored in a location of a data structure so that the location can be returned by a kernel driver to a translation node, as required by claim 1.

Appeal Br. 6.

The Examiner finds that Tsirkin's kernel-based hypervisor 125 (the claimed "kernel driver") stores mappings of host device ID, bus address, host physical address, and access rights of allocated memory pages (the claimed "memory allocation information") within the host mapping of the host IOMMU (the claimed "data structure"). Ans. 14–17; Tsirkin ¶¶ 32, 36, 48; Final Act. 5–6. According to the Examiner, these features of Tsirkin disclose the claim limitation "wherein the kernel driver . . . store[s] memory allocation information about the allocation of host memory in a data structure." *Id.*

The Examiner further finds that Tsirkin's kernel-based hypervisor 125 returns the bus address, which is a location of the host physical addresses of the pages as provided within the Host IOMMU/host mapping (the claimed "memory allocation information in the data structure"), to the emulated IOMMU (the claimed "translation node") upon determining the allocation and location of the host physical address of the physical memory pages. *Id.* The Examiner finds that these Tsirkin features disclose the claimed "return a location of the memory allocation information in the data structure to the translation node." *Id.*

Alternatively, the Examiner finds that Tsirkin's memory pages belonging to the Guest OS are the claimed "memory allocation information" and that the bus address is again in this mapping the claimed "location of the memory allocation information in the data structure." Ans. 17–18; Tsirkin ¶¶ 36, 46; Final Act. 5–6.

Claims are given their broadest *reasonable* interpretation consistent with the specification in which they appear. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (emphasis added). In both

alternative mappings, the Examiner has interpreted Tsirkin's bus address as the claimed "location of the memory allocation information." Ans. 14–15, 17–18. Tsirkin discloses that the bus address may include a base address that indicates where a DMA buffer starts, and an offset that indicates the size of the DMA buffer. Tsirkin ¶ 36. Thus, Tsirkin's bus address is not a location in a data structure that stores information about the allocation of host memory, as claimed: rather, it is the base address of a DMA buffer used to transfer data between a device and computer. We find the Examiner errs by interpreting "memory allocation information" too broadly to encompass Tsirkin's bus address for reasons Appellant provides. *See* Appeal Br. 6, *supra*. The Examiner does not rely on Suzuki or any of the remaining references to disclose this claim feature.

Accordingly, the Examiner errs in finding the reference combinations, and particularly Tsirkin, discloses the argued claim feature. Thus, we do not sustain the obviousness rejection of claims 1–3, 5, 6, 10–12, and 14, which we have grouped together in our analysis.

Our decision on the argument addressed above is dispositive of the obviousness rejections of claims 1–3, 5, 6, 10–12, and 14, so we do not reach Appellant's remaining arguments.

Obviousness Rejection of Claims 4 and 13

Claims 4 and 13 depend from respective independent claims 1 and 10. Appellant argues for patentability of claims 4 and 13 on the same basis as claims 1 and 10. Appeal Br. 8. The Examiner relies on Schug to teach using "mmap" to map memory information. Final Act. 9–11. The Examiner does not rely on Schug to overcome the deficiencies of Tsirkin and Suzuki. Final

Act. 9–11. Accordingly, we reverse the rejection of claims 4 and 13 for the same reasons as stated for claims 1 and 10.

Obviousness Rejection of Claims 7–9 and 15–17

Claims 7–9 and 15–17 depend from respective independent claims 1 and 10. Appellant argues for patentability of claims 7–9 and 15–17 on the same basis as claims 1 and 10. Appeal Br. 8. In this rejection, the Examiner relies on Dong to teach performing a guest read process and host read process, and does not rely on Dong to overcome the deficiencies of Tsirkin and Suzuki noted with respect to claims 1 and 10. Final Act. 9–11. Accordingly, we reverse the rejection of claims 7–9 and 15–17 for the same reasons stated for claims 1 and 10.

CONCLUSION

The Examiner's rejections of claims 1–17 under 35 U.S.C. § 103 are reversed.

Claims Rejected	**35 U.S.C. §**	**References**	**Affirmed**	**Reversed**
1–3, 5, 6, 10–12, 14	103	Tsirkin, Suzuki		1–3, 5, 6, 10–12, 14
4, 13	103	Tsirkin, Suzuki, Schug		4, 13
7–9, 15–17	103	Tsirkin, Suzuki, Dong		7–9, 15–17
Overall Outcome				1–17

REVERSED