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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/983,729	12/30/2015	Semih Serbetli	81644620US03	4692

65913 7590 01/03/2019
Intellectual Property and Licensing
NXP B.V.
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EXAMINER

CHASE, SHELLY A

ART UNIT	PAPER NUMBER
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2112

NOTIFICATION DATE	DELIVERY MODE
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01/03/2019

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SEMIH SERBETLI and MARINUS VAN SPLUNTER

Appeal 2018-005669
Application 14/983,729
Technology Center 2100

Before CARLA M. KRIVAK, HUNG H. BUI, and JON M. JURGOVAN,
Administrative Patent Judges.

BUI, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellants seek our review under 35 U.S.C. § 134(a) from the Examiner’s Final Rejection of claims 1–13 and 15–19, which are all the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.¹

¹ Our Decision refers to Appellants’ Appeal Brief (“App. Br.”) filed November 21, 2017; Reply Brief (“Reply Br.”) filed May 10, 2018; Examiner’s Answer (“Ans.”) mailed March 22, 2018; Final Office Action (“Final Act.”) mailed August 8, 2017; and original Specification (“Spec.”) filed December 30, 2015.

STATEMENT OF THE CASE

Appellants' invention relates to a receiver chip and a method for "processing a signal by non-uniform quantization of log likelihood ratios" by determining a log likelihood ratio (LLR) value for each signal bit, quantizing the bits' LLR values into "quantization bins, each quantization bin having: a width representative of one or more LLR values[,] and an index value having a bit length," and associating each bit with the index value that corresponds to its LLR value, "the width of each quantization bin . . . [being] non-uniform." Spec. 3:28–4:4, 6:24–25; Abstract.

Claims 1 and 16 are independent. Representative claim 1 is reproduced below:

1. A method of processing and decoding data that is represented by a signal carried out by receiver circuitry, the method comprising:
 - first circuitry carrying out the steps of
 - receiving a plurality of bits,
 - calculating a log likelihood ratio, known as a LLR, for each bit,
 - providing a LLR value for each bit based on the calculated LLR, and quantizing the LLR values into a plurality of quantization bins based on at least one of a probability density of LLR values and a range of LLR values,
 - each quantization bin having
 - a width representative of one or more LLR values, and
 - an index value having a bit length; and
 - second circuitry carrying out the steps of associating each bit with the index value that corresponds to its LLR value, and in response generating decoded output data as derived from the signal,
- wherein the width of each quantization bin is non-uniform.

App. Br. 15–19 (Claims App’x).

EXAMINER’S REJECTION²

Claims 1–13 and 15–19 stand rejected under 35 U.S.C. § 101 because the claimed invention is directed to an abstract idea without significantly more. Final Act. 3–4; Ans. 3–5.³

ANALYSIS

In *Alice Corp. Pty. Ltd. v. CLS Bank International*, 134 S. Ct. 2347 (2014), the Supreme Court reiterates an analytical two-step framework previously set forth in *Mayo Collaborative Services v. Prometheus Laboratories, Inc.*, 566 U.S. 66, 79 (2012), “for distinguishing patents that claim laws of nature, natural phenomena, and abstract ideas from those that claim patent-eligible applications of those concepts.” *Alice*, 134 S. Ct. at 2355. The first step in the analysis is to “determine whether the claims at issue are directed to one of those patent-ineligible concepts,” such as an abstract idea. *Id.* If the claims are directed to eligible subject matter, the inquiry ends. *Thales Visionix Inc. v. United States*, 850 F.3d 1343, 1349

² Claims 16, 17, and 19 were rejected under 35 U.S.C. § 112(b), as being indefinite. Final Act. 3. However, this rejection was withdrawn in the Examiner’s Answer, and is no longer pending on appeal. Ans. 3.

³ The Final Action rejects the claims as “directed to a mathematical algorithm[]” like the claims in *Gottschalk v. Benson*, 409 U.S. 63, 67 (1972). Final Act. 4. A new ground of rejection, presented for the first time in the Examiner’s Answer, rejects the claims as “directed to the abstract idea of a concept of tracking or organization of information” (emphasis omitted). Ans. 3–5 (“NEW GROUNDS OF REJECTION”).

(Fed. Cir. 2017); *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1339 (Fed. Cir. 2016).

If the claims are directed to a patent-ineligible concept, the second step in the analysis is to consider the elements of the claims “individually and ‘as an ordered combination’” to determine whether there are additional elements that “‘transform the nature of the claim’ into a patent-eligible application.” *Alice*, 134 S. Ct. at 2355 (citing *Mayo*, 566 U.S. at 79, 78). In other words, the second step is to “search for an ‘inventive concept’—*i.e.*, an element or combination of elements that is ‘sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [ineligible concept] itself.’” *Id.* (citing *Mayo*, 566 U.S. at 72–73). “[W]ell-understood, routine, [and] conventional activit[ies]’ previously known to the industry” are insufficient to transform an abstract idea into patent-eligible subject matter. *Id.* at 2359 (quoting *Mayo*, 566 U.S. at 73).

In rejecting claims 1–13 and 15–19 under 35 U.S.C. § 101, the Examiner determines these claims are directed to (i) a mathematical algorithm and performing mathematical calculations, similar to the claims of *Benson* (Final Act. 4; Ans. 7, 10), and (ii) an “abstract idea of a concept of tracking or organization of information” similar to the claims in *RecogniCorp, LLC v. Nintendo Co.*, 855 F.3d 1322 (Fed. Cir. 2017) (Ans. 3–4). The Examiner also determines

[t]he claim(s) does/do not include additional elements that are sufficient to amount to significantly more than the judicial exception because the addition of the first circuitry and the second circuitry does not change the deficiency of the claim since the first circuitry and second circuitry are for the purpose of the abstract idea.

Final Act. 4.

Appellants argue claims 2–12 and 15–19 together with claim 1. Reply Br. 2–4; App. Br. 4, 10, and 12. We select claim 1 as representative. Claims 2–12 and 15–19 stand or fall with claim 1 (*see* 37 C.F.R. § 41.37(c)(1)(iv)).

Alice/Mayo—Step 1 (Abstract Idea)

Turning to the first step of the *Alice* inquiry, Appellants contend claim 1 is not directed to an abstract idea because the claim “solves an important issue with the prior art, that is high memory requirement in processing LLRs through the use of non-uniform quantization bins” and “recites a novel method of decoding a signal using significant less memory resources.” Reply Br. 3–4; App. Br. 6–7. Appellants also argue the Examiner’s finding the claim “directed to the concept of tracking or organizing information” overgeneralized the claim. Reply Br. 6.

Appellants’ arguments are persuasive only in part. Particularly, we agree with Appellants that independent claims 1 and 16 are not “directed to the abstract idea of a concept of tracking or organization of information” as asserted by the Examiner. *See* Ans. 3. While we do not agree with the Examiner that the claims recite the concept of tracking and organizing information, we agree with the Examiner that the claims recite steps of a mathematical algorithm, similar to the claims in *Benson*. Final Act. 4; Ans. 6–7, 10. The claim language, in light of the Specification, supports the Examiner’s determination that the claims are directed to an abstract idea. Ans. 7; Final Act. 4. Particularly, the instructions recited in claims 1 and 16 group LLR values into groups of varying granularity (“quantization bins”), some bins including more LLR values (e.g., a bin includes four LLR values of -14, -13, -12, and -11, *see* Spec. 14, Table 1), other bins including fewer LLR values (e.g., a bin includes two LLR values of -7 and -6, *see* Table 1).

Claims 1 and 16 then associate each bin’s LLR values with an “index value,” the index value being an average or approximation of the bin’s LLR values—e.g., associate the four LLR values (-14, -13, -12, and -11) with one “index value” of -12, and associate the two LLR values (-7 and -6) with one “index value” of -6. *See* Spec. 14:5–15, Table 1. The index values (e.g., -12 and -6) are then represented by 4-bit values (e.g., 0001 and 0011). *See* Spec. 14:11–15, Table 1. Thus, similar to *Benson*, claims 1 and 16 recite steps of a mathematical algorithm manipulating particular values. *See Benson*, 409 U.S. at 65, 67; *see also In re Grams*, 888 F.2d 835, 837 (Fed. Cir. 1989) (“[M]athematical algorithms join the list of non-patentable subject matter not within the scope of section 101.”).

Therefore, we are not persuaded that the Examiner erred in determining claims 1 and 16 are directed to an abstract idea under step one of the *Alice* framework.

Alice/Mayo—Step 2 (Inventive Concept)

In the second step of the *Alice* inquiry, Appellants argue, the claims recite significantly more than an abstract idea because the claims are useful for “processing wireless data reception to reduce memory requirements in . . . [a] data processing system” and reducing a “high memory requirement in processing LLRs through the use of non-uniform quantization bins.” App. Br. 7, 12; Reply Br. 2, 6–8. We agree with Appellants that claims 1 and 16 recite additional limitations that amount to significantly more than the abstract idea, the additional limitations reciting a specific application of the mathematical algorithm that improves the functioning of a signal decoder/receiver. App. Br. 7, 12; Reply Br. 2, 6. Particularly, as discussed by the Federal Circuit in *Bascom*, “an inventive concept can be found in the

ordered combination of claim limitations that transform the abstract idea of filtering content into a particular, practical application of that abstract idea.” See *Bascom Global Internet Services, Inc. v. AT&T Mobility LLC*, 827 F.3d 1341, 1352 (Fed. Cir. 2016). We find Appellants’ incorporation of circuitry that “quantiz[es] the LLR values into a plurality of quantization bins,” “each quantization bin having a width representative of one or more LLR values, and an index value having a bit length” and “the width of each quantization bin is non-uniform” sufficiently transforms the abstract idea (i.e., manipulating LLR values by an algorithm) into “a particular, practical application of that abstract idea,” as discussed by the Federal Circuit in *Bascom* (827 F.3d at 1352).

Our conclusion is supported by Appellants’ Specification, which explains, “[b]y utilising non-uniform width bins during quantization of the LLR values, the width of each bin may be tailored according to the fidelity of the incoming signal,” the “[u]se of non-uniform quantization/compression to represent the LLRs . . . allow[ing] for a greater compression efficiency with limited number of bits.” See Spec. 4:5–15. When implemented in a signal decoder/receiver, Appellants’ LLR compression algorithm results in “reduced cost on memory and/or a reduced cost of sending the LLRs to another system for channel decoding,” and savings in the amount of memory space required to store and process LLRs for decoding the signal (for which the LLRs indicate likelihood of noise distortion). See Spec. 3:24–26, 11:6–8, 19:2–11. Thus, taking all the claim elements both individually and as an ordered combination, claims 1 and 16 as a whole amount to significantly more than the mathematical algorithm. *Alice*, 134 S. Ct. at 2357. Accordingly, we do not sustain the Examiner’s rejection of claims 1–12 and

15–19 under 35 U.S.C. § 101.^{4 5} We also do not sustain the Examiner’s rejection of dependent claim 13 under 35 U.S.C. § 101 because claim 13 incorporates additional storage and decoding limitations in a “practical application of . . . [the] abstract idea.” *See Bascom*, 827 F.3d at 1352.

CONCLUSION

On the record before us, we conclude Appellants have demonstrated the Examiner erred in rejecting claims 1–13 and 15–19 under 35 U.S.C. § 101.

⁴ In the event of further prosecution, we recommend the Examiner consider rejecting independent claim 1 under 35 U.S.C. § 112(b), as being indefinite and incomplete because the claim is unclear as to: (1) any relationship between the claimed “receiver circuitry” and the claimed “first circuitry” and “second circuitry”; and (2) any relationship between the claimed “signal” and the claimed “plurality of bits” received by the first circuitry and associated with index values by the second circuitry. Regarding issue (1), the claim merely recites a method performed by the first and second circuitry without indicating whether the first and circuit circuitry are associated in any way with the claimed “receiver circuitry.” Regarding issue (2), the claim merely recites processing the “plurality of bits” without indicating any relationship between these “bits” and the claimed “data that is represented by a signal” or the claimed “decoded output data as derived from the signal.”

⁵ In the event of further prosecution, we recommend the Examiner consider rejecting independent claim 16 under 35 U.S.C. § 112(b), as being indefinite and incomplete because the claim does not specify *any end result* of “quantizing the LLR values into a plurality of quantization bins” and “associat[ing] each bit with the index value that corresponds to its LLR value.” As currently written, claim 16 merely requires “[a] receiver responsive to a received signal having a plurality of bits,” which does not specify any output or end result obtained by the claimed receiver.

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DECISION

As such, we REVERSE the Examiner's rejection of claims 1–13 and 15–19 under 35 U.S.C. § 101.

REVERSED