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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte THOMAS KERN, JENS ROSENBUSCH, ULRICH BACKHAUSEN, and THOMAS NIRSCHL[1]

Appeal 2018-005347
Application 13/966,679
Technology Center 2100

Before JEAN R. HOMERE, JAMES B. ARPIN, and SHARON FENICK, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants seek our review under 35 U.S.C. § 134(a) of the Examiner's final decision rejecting claims 1–15, 18, and 19, all of the claims pending in the application. Final Act. 1.[2] Claims 16 and 17 are cancelled,

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[1] According to Appellants, Infineon Technologies AG is the real party-in-interest. App. Br. 1.

[2] In this Decision, we refer to Appellants' Appeal Brief, filed June 2, 2017 ("App. Br.") and Reply Brief, filed April 23, 2018 ("Reply Br."); the Final Office Action, mailed December 12, 2016 ("Final Act."); the Examiner's Answer, mailed February 27, 2018 ("Ans."); and the Specification, filed August 14, 2013 ("Spec."). Rather than repeat the Examiner's findings and

and claims 20–21 are withdrawn from consideration as directed to an unelected invention. *Id.* at 2; App. Br. 16–17 (Claims App'x). We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

STATEMENT OF THE CASE

Appellants' invention relates to

> A memory system having a flexible read reference is disclosed. The system includes a memory [partition], a failcount component, and a controller. The memory partition includes a plurality of memory cells. The failcount component is configured to generate failcounts in response to read operations of the memory [partition]. The controller is configured to calibrate a reference value for the memory partition by utilizing the failcounts.

Spec. Abstract. "[T]he calibrated reference value is compared with a cell state voltage to determine a cell state." App. Br. 14 (Claims App'x, claim 1); *see id.* at 16 (Claims App'x, claim 13). Further, Appellants' invention relates to calibrating methods, in which a reference value is set and then, for example, sequentially decreased by a step amount until a step limit is reached and a failcount exceeds a fail limit. The last modified reference value then is compared with a read cell state voltage. Spec. ¶¶ 25–35, Fig. 4; *see id.* ¶ 14.

Claims 1 and 13 are independent and are directed to a memory system and a calibrating method, respectively. App. Br. 14–16 (Claims App'x). Claims 2–12 depend directly or indirectly from claim 1; and claims 14, 15,

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determinations and Appellants' contentions in their entirety, we refer to these documents.

18, and 19 depend directly or indirectly from claim 13. *Id.* Claim 1, reproduced below, is illustrative.

> 1. A memory system utilizing a flexible read reference, the system comprising:
>
> a memory partition having a plurality of memory cells, wherein each cell has a cell state voltage based on a read operation;
>
> a failcount component configured to generate failcounts in response to read operations of the memory partition, where the failcounts indicate a number of the memory cells having failed reads; and
>
> *a controller configured to generate a calibrated reference value for read operations* of the memory partition by utilizing the failcounts from the failcount component, *wherein* the controller is configured to generate the calibrated reference value by sequentially reducing a modified reference value until the failcount exceeds a fail limit to obtain the calibrated reference value, wherein the modified reference value starts at an initial value, *wherein the calibrated reference value is compared with a cell state voltage to determine a cell state*.

App. Br. 14 (Claim App'x) (disputed limitations emphasized).

REFERENCES AND REJECTIONS

The Examiner relies upon the following prior art in rejecting the pending claims:

Name	Pat./Publ. No.	Issue/Publ. Date	Filing Date
Sevugapandian	US 8,996,936 B2	Mar. 31, 2015; June 13, 2013	Jan. 23, 2012
Kochar *et al.* ("Kochar")	US 2014/0258590 A1	Sept. 11, 2014	Mar. 7, 2013
Matsunaga	US 2013/0148435 A1	June 13, 2013	June 25, 2012
Paparisto *et al.* ("Paparisto")	US 7,379,339 B2	May 27, 2008; June 15, 2006	Nov. 16, 2005
Frankowsky *et al.* ("Frankowsky")	U.S. 6,603,694 B1	Aug. 5, 2003	Feb. 5, 2002

Claims 1–3, 5, 6, and 8–12 stand rejected as unpatentable under 35 U.S.C. § 103 over the combined teachings of Kochar and Matsunaga.[3] App. Br. 3. Claims 13–15, 18, and 19 stand rejected as unpatentable under 35 U.S.C. § 103 over the combined teachings of Kochar, Matsunaga, and Frankowsky. *Id.* Claim 4 stands rejected as unpatentable under 35 U.S.C. § 103 over the combined teachings of Kochar, Matsunaga, and Paparisto. *Id.* Claim 7 stands rejected as unpatentable under 35 U.S.C. § 103 over the combined teachings of Kochar, Matsunaga, and Sevugapandian. *Id.*

We review the appealed rejections for error based upon the issues identified by Appellants, and in light of the arguments and evidence

[3] *See In re Bush*, 296 F.2d 491, 496 (CCPA 1961) ("where a rejection is predicated on two references each containing pertinent disclosure which has been pointed out to the applicant, we deem it to be of no significance, but merely a matter of exposition, that the rejection is stated to be on A in view of B instead of on B in view of A, or to term one reference primary and the other secondary.").

produced thereon. *Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential). Arguments not made are waived. *See* 37 C.F.R. § 41.37(c)(1)(iv) (2017).

ANALYSIS

Issue: Does the Examiner err in finding the combined teachings of Kochar and Matsunaga teach or suggest "the calibrated reference value is compared with a cell state voltage to determine a cell state," as recited in claim 1? *See id.* at 16 (Claim App'x, claim 13: "performing one or more read operations to determine a cell state by comparing a read cell state voltage with the calibrated reference value").

The Examiner finds Matsunaga teaches the limitation at issue. *See* Final Act. 5; Ans. 2–4 (citing Matsunaga, Figs. 2A, 2B, 3). The Examiner relies on Matsunaga's discussion of a diagram showing a threshold distribution of a plurality of memory cells, i.e., Figure 12, in which "the analog voltage shown for '00' is compared with VC to determine that the cell contents are '00'." Final Act. 5 (citing Matsunaga, Fig. 12); *see* Matsunaga ¶¶ 116–117.

Matsunaga teaches, in performing a read operation from a memory, "a voltage value to be read from memory cells changes due to number of writing/erasure [sic], a data retaining period, and a surrounding temperature." Matsunaga ¶ 3. Matsunaga's Figure 12 is reproduced below.

FIG.12

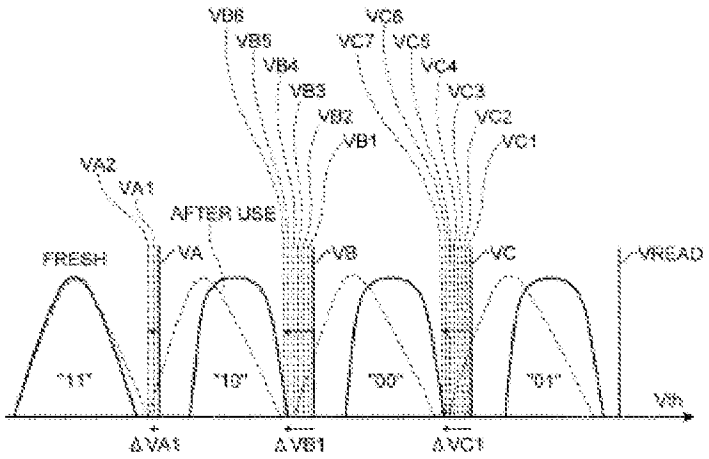

Figure 12 depicts

> a degree of decrease in the threshold distribution may differ among data. For example, for data "10", the read voltage is gradually shifted from VA to VA1 and then VA2, and the reading succeeds with the read voltage VA2. The reading number of the data "10" is for example *2*. . . .
>
> Alternatively, a changing amount of the read voltage with which the reading of the data "10" had succeeded from a default value is *ΔVA1*.

Id. ¶¶ 116–117 (emphases added).

Matsunaga's Figure 2A also is reproduced below.

FIG.2A

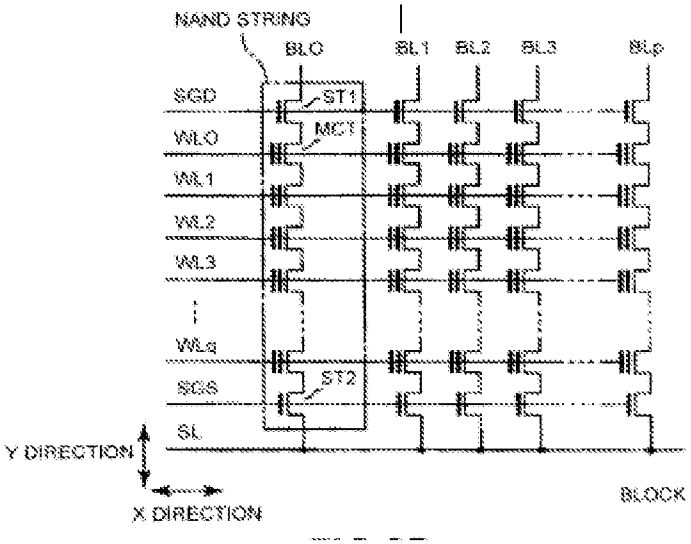

Figure 2A depicts a circuit diagram showing an example of a configuration of a physical block included in the NAND memory. *Id.* ¶¶ 5, 43.

Matsunaga explains that:

> The word lines WL0 to WLq commonly connect the control gate electrodes of the memory cell transistors MCT between the NAND strings in the physical block. That is, the control gate electrodes of the memory cell transistors MCT [(also referred to as a memory cell)] *that are in the same row in a block are connected to the same word line WL.*

Id. ¶ 48 (emphasis added). Matsunaga also explains, "the bit lines BL0 to BLp commonly connect the drains of the select transistors ST1 between blocks. That is, the NAND strings *in the same column in the blocks are connected to the same bit line BL.*" *Id.* ¶ 49 (emphasis added). Matsunaga describes that:

> The non-volatile memory includes a plurality of memory cells driven by word lines and a voltage generating section that generates a read voltage to be applied to the word lines. *The monitoring section monitors a change in a threshold distribution of the plurality of memory cells upon performing a read*

> *processing to read data from the plurality of memory cells by applying the read voltage to the word lines.*

Id. ¶ 26 (emphasis added). However, referring to Figure 12, whether the reading number or a read voltage changing amount is determined, the value is determined with respect to the read voltage of the word line. *Id.* ¶¶ 116–117.

Appellants dispute the Examiner's findings and contend that Matsunaga does not teach "the calibrated reference value is compared with a cell state voltage to determine a cell state," as recited in claim 1. App. Br. 4–6; Reply Br. 3–4. Referring to Figure 1, the Specification explains:

> The cells within the memory partition 104 have at least a first state and a second state. However, it is appreciated that the cells can have more than two states, also referred to as multilevel cells. *Each state has a threshold value, referred to as a cell state voltage, which is read during read operations using a sense current which generates a read current or a cell state current.* The read current, corresponds to the state threshold value, and is compared with the reference current 112 to yield the state or state values. *For example, a binary memory cell may yield a value of '0' for state read current above the reference current and a value of '1' for state read current below the reference current 112.*

Spec. ¶ 9 (emphases added). Specifically, Appellants contend that bit line voltage, rather than word line voltage, corresponds to the cell state voltage. App. Br. 4–6. Thus, referring to Matsunaga's Figure 12, Appellants conclude

> the read voltage that is sequentially altered and allegedly corresponds to the calibrated reference value is the wordline voltage applied to the cell to address the cell for a subsequent read operation. This read voltage (*i.e.*, wordline voltage) is not a calibrated reference value ***that is compared with a cell state voltage*** (*e.g.*, bitline voltage across the memory cell) as recited in claim 1.

App. Br. 6 (citing Matsunaga ¶¶ 26, 68, 165). We agree.

The Examiner argues that the definition of a "cell state voltage" proposed by Appellants was not present in the Specification and constitutes new matter. Ans. 2 (citing App. Br. 4–5). We disagree for two reasons. First, we find the Specification, quoted above, provides an express definition of "cell state voltage." Spec. ¶ 9. Second, although the Specification does not mention *word lines* or *bit lines*, Appellants contend "[t]his conventional memory cell operation is well understood by one of ordinary skill in view of applicant[s'] specification, particularly in view of paragraph [9]." App. Br. 6. We find this contention persuasive. *See* Matsunaga ¶¶ 48, 49; Kochar ¶ 23; Sevugapandian, 3:15–38; *see also Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) ("the level of skill in the art is a prism or lens through which a judge, jury, or the Board views *the prior art and the claimed invention*" (emphasis added)).

The Examiner also argues that, given the broadest reasonable interpretation of the terms "calibrated reference value" and "cell state voltage," these claim terms are taught by Matsunaga. Ans. 3–4. However, the Examiner does not interpret expressly those claim terms. *Id.* at 2–3. Thus, we are not persuaded by the Examiner's arguments regarding the undefined scope of these terms.

Appellants contend that the "alleged calibrated reference value (VA1-VA2) of [Matsunaga's Figure 12] is *never compared* to a cell state voltage as in claim 1 and is *never used* to determine the cell state." Reply Br. 3. Instead, as noted above, Matsunaga teaches monitoring word line voltages "to determine the life or remaining life of the block of cells." *Id.* at 3–4; *see* Matsunaga ¶¶ 3, 26, 113–117. The problems to be solved by the recited

systems and methods and those taught by Matsunaga differ. *Compare* Spec. ¶¶ 1, 2, 9–14 *with* Matsunaga Abstract, ¶¶ 3, 26; *see* Kochar ¶ 32. Thus, the voltages read by the recited systems and methods and those read by Matsunaga understandably differ too. We find Appellants' contention persuasive because, to the extent that Matsunaga teaches or suggests a calibrated reference value, that value is not shown to be "*compared* with a cell state voltage *to determine a cell state*," as recited in claim 1. Appellants also contend that, to the extent that Matsunaga fails to teach or suggest using the calibrated reference value for comparison with a cell state voltage to determine a cell state, Matsunaga also fails to teach or suggest a controller configured to generate such "a calibrated reference value for read operations," as recited in claim 1. Final Act. 5; *but see* App. Br. 7–10. For the reasons set forth above, we agree with Appellants. Thus, we also do not agree with the Examiner's finding that Matsunaga teaches or suggests "performing one or more read operations to determine a cell state by comparing a read cell state voltage with the calibrated reference value," as recited in claim 13. Final Act. 8; *but see* App. Br. 11.

For the reasons discussed above, Appellants have shown error in the Examiner's factual findings and conclusion of obviousness. Accordingly, we do not sustain the Examiner's 35 U.S.C. § 103 rejection of independent claims 1 and 13. *See* App. Br. 4–7, 11. Dependent claims 2–12, 14, 15, 18, and 19 are not argued separately, but the rejections of those claims are not sustained for the same reasons given for independent claims 1 and 13. *See* App. Br. 10 (claims 2, 3, 5, 6, and 8–12), 11 (claims 14, 15, 18, and 19), 12 (claims 4 and 7).

DECISION

We reverse the Examiner's decision rejecting claims 1–15, 18, and 19.

REVERSED