UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/504,637	10/02/2014	Philip J. Agar	2013P-180-US (1506.485)	1024

63122 7590 02/27/2020

ROCKWELL AUTOMATION, INC./BF
ATTENTION: Linda Kasulke
1201 SOUTH SECOND STREET
MILWAUKEE, WI 53204

EXAMINER
FOTAKIS, ARISTOCRATIS

ART UNIT	PAPER NUMBER
2633	

NOTIFICATION DATE	DELIVERY MODE
02/27/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@boylefred.com
raintellectualproperty@ra.rockwell.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PHILIP J. AGAR and ALISON COOPER

Appeal 2018-005325
Application 14/504,637[1]
Technology Center 2600

Before JOSEPH L. DIXON, HUNG H. BUI, and JON M. JURGOVAN, *Administrative Patent Judges*.

BUI, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant seeks our review under 35 U.S.C. § 134(a) from the Examiner's Final rejection of claims 1–20, which are all the claims pending in the application. Appeal Br. 14–17, Claims App. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.[2]

---

[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. The real party in interest is Rockwell Automation Limited. Appeal Br. 3.

[2] Our Decision refers to Appellant's Appeal Brief filed November 27, 2017 ("Appeal Br."); Reply Brief filed April 12, 2018 ("Reply Br."); Examiner's Answer mailed March 7, 2018 ("Ans."); the Final Office Action mailed July 13, 2017 ("Final Act."); and the original Specification filed October 2, 2014 ("Spec.").

STATEMENT OF THE CASE

Appellant's invention is directed to a method and apparatus for processing electrical signals having encoded digital signals such as "a frequency modulated signal encoding digital data," by "sampling a first portion of the electrical signal to provide a first sample set," "determining an intermediate value from the first sample set," and selecting "[a] first output value . . . from a plurality of stored output values based on the intermediate value, the output value indicating a frequency modulation encoded value within the first portion of the electrical signal." Spec. ¶ 2; Abstract.

Claims 1 and 15 are independent. Independent claim 1, reproduced below, is exemplary of the subject matter on appeal.

> 1. A method for processing an electrical signal comprising:
>
> receiving an electrical signal comprising a frequency modulated signal encoding digital data;
>
> obtaining a plurality of samples of a first portion of the electrical signal, wherein each sample corresponds to an amplitude of the electrical signal and each sample in the plurality of samples occurs at a sample time different than the sample time of the other samples in the plurality of samples;
>
> generating a first value if the amplitude of the electrical signal is greater than a threshold;
>
> generating a second value if the amplitude of the electrical signal is less than the threshold;
>
> storing a plurality of values, wherein each of the plurality of values is one of the first value and the second value and wherein each of the plurality of values corresponds to one sample selected from the plurality of samples and to the corresponding sample time to generate a first sample set, wherein each of the plurality of values in the first sample set corresponds to a different sample time;
>
> using a sliding window having a predefined number of values to generate an intermediate value from the first sample

set, wherein the intermediate value is updated at each sample time;

obtaining a first output value from a table of output values wherein:

the intermediate value is an index into the table of output values,

the first output value is read from a position in the table of output values corresponding to the intermediate value, and

the first output value indicates a frequency modulation encoded value within the first portion of the electrical signal; and

outputting an indication of the first output value.

Appeal Br. 14 (Claims App.).

Evidence Considered

Name	Reference	Date
Lee et al. ("Lee")	US 5,818,296	Oct. 6, 1998
Liu	US 6,785,347 B1	Aug. 31, 2004
Golborne et al. ("Golborne")	US 2009/0168857 A1	July 2, 2009
Shelburne	US 2011/0286542 A1	Nov. 24, 2011
Chmelar et al. ("Chmelar")	US 2013/0243107 A1	Sept. 19, 2013

Examiner's Rejections

(1) Claims 1–3, 12, and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, and Liu. Final Act. 3–6.

(2) Claims 4–11 and 16–20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, Liu, and Golborne. Final Act. 6–10.

(3) Claims 13 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, Liu, and Lee. Final Act. 10–11.

ANALYSIS

With respect to claim 1, Appellant contends the Examiner erred in finding Chmelar discloses "storing a plurality of values, wherein each of the plurality of values is one of the first value and the second value and wherein each of the plurality of values corresponds to one sample selected from the plurality of samples and to the corresponding sample time" because (i) "'each of the plurality of values' disclosed by Chmelar corresponds to three samples rather than one sample as required by claim 1" and (ii) "Chmelar fails to disclose storing each of the plurality of values." Appeal Br. 11. Appellant also argues the Examiner's combination of Shelburne and Chmelar is improper because (i) there is insufficient rationale to combine the references and (ii) "[e]ven if Chmelar is combined with Shelburne, the proposed combination would render Shelburne entirely unsatisfactory for its intended purpose and would change the principle of operation of [Shelburne]." Appeal Br. 10; Reply Br. 2–6. We do not agree.

We agree with and adopt the Examiner's findings as our own. Ans. 3–7; Final Act. 6–10. Particularly, we agree with the Examiner that Chmelar *stores* the plurality of first and second values (e.g., a bit sequence b_{-3}, b_{-2}, b_{-1}, etc., of 0s and 1s shown in Figure 11A) generated with respect to a threshold (also shown in Figure 11A). Final Act. 5 (citing Chmelar ¶¶ 63–64, Fig. 11A); Ans. 6–7. For example, Chmelar discloses that bits b_k are stored by latches. *See* Chmelar ¶¶ 45 ("[l]atches 508 and 510 are used to store prior bits corresponding to each tap (e.g., $b_{-2}b_{-1}$)"), ¶ 51 ("the purpose of each latch [in Figure 8] is to provide storage for a corresponding bit for a bit

period in pipeline stages while predictive DFE [(decision feedback equalizer)] 800 is processing bits"); *see also* Chmelar ¶ 23 (explaining that "FIGS. 11A and 11B show an exemplary plot of comparator threshold voltages for the interleaved and retimed predictive selection DFE of FIG. 8").

We also agree with the Examiner that Chmelar teaches "each of the plurality of values corresponds to one sample selected from the plurality of samples and to the corresponding sample time" as recited in claim 1. Ans. 7; Final Act. 5. As the Examiner explains, "[t]he claim recites '[] *wherein <u>each</u> of the plurality of values corresponds to one sample*'" and "Chmelar clearly teaches that 'each of the plurality of values (three values, b_{-3}, b_{-2} and b_{-1})' corresponds to one sample (of the three samples) as required by claim 1, since each value corresponds to a particular sample." Ans. 7.

We are not persuaded by Appellant's argument that "'each of the plurality of values' disclosed by Chmelar corresponds to three samples rather than one sample" because "Fig. 11a and the associated discussion [in Chmelar] clearly indicate that multiple prior bits (b-2, b-2, and b-1) and the corresponding voltage levels (h3, h2, and h1) are used to determine whether each bit should be a logic zero or a logic one." Appeal Br. 11 (citing Chmelar ¶ 66, Fig. 11A). Appellant's argument is unpersuasive because, although Chmelar's adaptive threshold ($Vref=h_3-h_2+h_1$) is determined from *three* ISI (intersymbol interference) components h_1, h_2, and h_3, a determined bit *value* b_k (e.g., cursor bit b_0) *corresponds to one sample* that is either above the threshold (making cursor bit b_0 to be a logical high, e.g., logic 1) or below the threshold (making cursor bit b_0 to be a logical low, e.g., logic 0). *See* Chmelar ¶¶ 63–64, 66, Fig. 11A; *see also* Chmelar ¶¶ 45, 51, 105.

> We, therefore, agree with the Examiner that Chmelar teaches:
>
> storing a plurality of values, wherein each of the plurality of values is one of the first value and the second value and wherein each of the plurality of values corresponds to one sample selected from the plurality of samples and to the corresponding sample time to generate a first sample set, wherein each of the plurality of values in the first sample set corresponds to a different sample time,

as recited in claim 1.

As to Appellant's argument that "there would be no motivation to combine Chmelar with Shelburne" (*see* Appeal Br. 8; Reply Br. 5), the Examiner has articulated sufficient reasoning for combining Chmelar's thresholding and digitization, with Shelburne's processing of an electrical signal carrying a frequency modulated signal encoding digital data, to effectively perform digital conversion to pulse values of logical highs and logical lows—a concern shared by Chmelar and Shelburne. Ans. 3, 5 (citing Shelburne ¶ 43, Fig. 5; Chmelar Figs. 11A–11B); Final Act. 5; *see also* Shelburne ¶¶ 44–45; Chmelar ¶¶ 51, 63–64. Appellant argues "one of ordinary skill in the art has no motivation to combine the disclosure of Chmelar with Shelburne" because Chmelar addresses a problem associated with very high frequency digital signals, while Shelburne pertains to analog and low frequency HART signals. Appeal Br. 8–9; Reply Br. 2–3. Appellant's argument is not persuasive because the Examiner's rejection does not rely on changing Shelburne's frequency range to fit Chmelar's range; and Chmelar's analog-to-digital conversion (thresholding) technique is applicable to Shelburne's FSK (frequency-shift keying) data signal. Ans. 3.

Appellant's arguments regarding changing Shelburne's principle of operation and rendering Shelburne unsatisfactory for its intended purpose are also unpersuasive. *See* Appeal Br. 10; Reply Br. 3–6. That is, Appellant asserts that if Chmelar's threshold detector were added to Shelburne, "[t]he receiver of Shelburne would no longer generate a pulse at a zero-crossing" and "not only does [Shelburne] lose the zero detection upon which the rest of the decoding algorithm [of Shelburne] is based, there is no longer a pulse width upon which Shelburne can rely to determine whether a zero or a one was received." Appeal Br. 10–11; *see also* Reply Br. 3–4. However, Appellant has provided insufficient evidence supporting their arguments. Additionally, the Examiner's combination of Shelburne and Chmelar does not require the receiver of Shelburne to "no longer generate a pulse at a zero-crossing" as Appellant argues. *See* Appeal Br. 10. Rather, the Examiner's combination provides for measuring pulse widths between Shelburne's zero-crossings at on- and off-times (as explained by Shelburne, *see* ¶¶ 23, 43–45 ("measure the pulse widths of the on- and off-times of the digital pulsed signal PLS [that is obtained by measuring the zero-crossings of FSK data signal FSK_DATA]")), by measuring durations of logical highs and logical lows obtained from Shelburne's FSK signal using Chmelar's thresholding. Ans. 3, 5. As the Examiner explains, "[i]ncorporating a threshold detection [of Chmelar] would <u>not</u> lose the zero detection upon which the rest of the decoding algorithm [of Shelburne] is based (as argued by Appellants) but instead it would detect the '1's and '0's of the signal," with the zero-crossing detection of Shelburne "detect[ing] the zero-crossings or edges of the pulses." Ans. 5.

We therefore are not persuaded by Appellant's arguments that (i) "there are no longer any zero crossings and the zero crossing detection of Shelburne fails," (ii) Shelburne would "lose the zero detection upon which the rest of the decoding algorithm is based," and (iii) "there is no longer a pulse width upon which Shelburne can rely to determine whether a zero or a one was received." *See* Appeal Br. 10–11; Reply Br. 4.

Appellant also argues Chmelar's analog-to-digital conversion would merely convert Shelburne's HART signal to a square wave whose "frequency . . . would determine whether a '1' or a '0' is present," which (i) "provides no benefit to Shelburne, as it is the *frequency* of the original analog signal *not an amplitude* (as may be identified by a threshold detector) that must also be detected to determine whether the HART signal includes a 'l' or a '0,'" and (ii) "creates an unnecessary step to the analog-to digital conversion disclosed by Shelburne." Reply Br. 4. Appellant's arguments are not persuasive because both Shelburne and Chmelar use voltage references to detect threshold crossings by signal amplitudes—*see*, *e.g.*, Shelburne's paragraph 44 describing "comparator 190 . . . configured as a zero-crossing detector" using a bias voltage for "detect[ing] zero-crossings of the FSK data signal FSK_DATA to generate the digital pulsed signal PLS," and Chmelar's Fig. 11A using voltage reference Vref. Appellant has provided attorney argument with insufficient evidence that (i) "insertion of the threshold detection [of Chmelar] creates an unnecessary step to the analog-to digital conversion disclosed by Shelburne," or that (ii) "addition of a threshold detector [of Chmelar] would cause the analog-to-digital converter disclosed by Shelburne to not function properly and would require

further modification to compensate for the improper frequency generated." *See* Reply Br. 4–5.

Thus, we agree with the Examiner's findings that Appellant has failed to clearly distinguish the claimed invention over the prior art relied on by the Examiner. We, therefore, sustain the Examiner's rejection of independent claim 1, independent claims 15 reciting similar limitations and argued for reasons similar to claim 1, and dependent claims 2–14 and 16–20 for which no separate arguments are provided. Appeal Br. 5, 12.

CONCLUSION

On the record before us, we conclude Appellant has not demonstrated the Examiner erred in rejecting: (1) claims 1–3, 12, and 15 under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, and Liu; (2) claims 4–11 and 16–20 under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, Liu, and Golborne; and (3) claims 13 and 14 under 35 U.S.C. § 103 as being unpatentable over Shelburne, Chmelar, Liu, and Lee.

DECISION SUMMARY

As such, we AFFIRM the Examiner's final rejection of claims 1–20 under 35 U.S.C. § 103.

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–3, 12, 15	103	Shelburne, Chmelar, Liu	1–3, 12, 15	

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
4–11, 16–20	103	Shelburne, Chmelar, Liu, Golborne	4–11, 16–20	
13, 14	103	Shelburne, Chmelar, Liu, Lee	13, 14	
Overall Outcome			1–20	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED