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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte AKSHAY MATHUR, DHARANI KOTTE, CHAYAN BISWAS, BASKARAN KANNAN, and SUMANT K. PATRO[1]

Appeal 2018–004947
Application 14/323,921
Technology Center 2100

Before CARL W. WHITEHEAD JR., JASON V. MORGAN and ERIC B. CHEN, *Administrative Patent Judges*.

WHITEHEAD JR., *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant is appealing the Examiner's Final rejection of claims 1–23 under 35 U.S.C. § 134(a). Appeal Brief 7. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

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[1] We use the word Appellant to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Sandisk Technologies LLC, as the real party in interest. Appeal Brief 5.

Introduction

According to Appellant, the invention "relate[s] generally to memory systems, and in particular, to using history I/O sizes and I/O sequences to trigger coalesced writes in a nonvolatile storage device." Specification ¶ 2.

Representative Claim

Claim 1, reproduced below, is illustrative of the claimed subject matter.

> 1. A method, comprising:
>
> receiving, at a storage device, a plurality of input/output (I/O) requests from a host, the plurality of I/O requests including read requests and write requests to be performed in a plurality of regions in a logical address space of the host; and
>
> performing one or more operations for each region of the plurality of regions in the logical address space of the host, including:
>
> determining whether the region has a history of I/O requests to access data, in the region in the logical address space of the host, of size less than a predefined small-size threshold during a predetermined time period;
>
> determining whether the region has a history of sequential write requests to the region in the logical address space of the host during the predetermined time period; and
>
> in accordance with a determination that the region has a history of I/O requests to access data of size less than a predefined small-size threshold during the predetermined time period and that the region has a history of sequential write requests during the predetermined time period, coalescing subsequent write requests to the region.

References

Name	Reference	Date
Palmer	US 2013/0007381 A1	January 3, 2013
Ng et al.	US 2013/0073784 A1	March 21, 2013
Fleischer et al.	US 2014/0173224 A1	June 19, 2014
Edmondson et al.	US 8,928,681 B1	January 6, 2015
Udayashankar et al.	US 2015/0032967 Al	January 29, 2015
Simionescu et al.	US 2015/0286438 A1	October 8, 2015

Rejections on Appeal

Claims 1, 3–8, 10–12, 15, 17, 19, 20 and 22 stand rejected under pre-AIA 35 U.S.C. § 103 as being unpatentable over Simionescu, Ng and Edmondson. Final Action 2–15.

Claims 2, 16 and 21 stand rejected under pre-AIA 35 U.S.C. § 103 as being unpatentable over Simionescu, Ng, Edmondson and Palmer. Final Action 15–17.

Claims 9, 18 and 23 stand rejected under pre-AIA 35 U.S.C. § 103 as being unpatentable over Simionescu, Ng, Edmondson and Udayashankar. Final Action 17–19.

Claims 13 and 14 stand rejected under pre-AIA 35 U.S.C. § 103 as being unpatentable over Simionescu, Ng, Edmondson and Fleischer. Final Action 19–20.

ANALYSIS[2]

Rather than reiterate the arguments of Appellant and the Examiner, we refer to the Appeal Brief (filed October 19, 2017), the Reply Brief (filed April 9, 2018), the Final Action (mailed April 20, 2017) and the Answer (mailed February 9, 2018), for the respective details.

Appellant argues, that "[i]n Simionescu, the mode of operation is changed for **all** of the write commands issued from the host computer to the storage device, as opposed to 'performing one or more operations **for each region** of the plurality of regions in the logical address space of the host' and making unique determinations for each region." Appeal Brief 15. It is noted that the Examiner relied upon Edmondson to disclose "performing one or more operations for each region of the plurality of regions in the logical address space of the host" and not Simionescu. Final Action 3–4. The Examiner finds:

> Simionescu does not disclose, but Ng discloses determining whether the region has a history of I/O requests to access data, in the region in the logical address space of the host, of size less than a predefined small-size threshold during a predetermined time period (e.g., unaligned data to cache portions of data from host data writes that contain data that do not make up a size of a complete bank page, 0019; a page is cells within a block containing minimum amount of data and a logical block includes logical block addresses (LBAs) with data received from host mapped to physical blocks, 0022).

Final Action 3.

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[2] Appellant argues the claims do not all stand and fall together but rather, for purposes of appeal, the claims are presented in three groups — Group A. (claims 1, 2, 5, 6, and 8–23); Group B. (claims 3 and 4) and Group C. (claim 7). *See* Appeal Brief 13 ("Elements common to these groups will be discussed together.").

Appellant contends, "regarding Ng, there is a fundamental difference between[] always writing data unaligned with a physical page boundary in a separate queue from page aligned data, and . . . determining whether a region of memory has '**a history of I/O requests to access data of size less than a predefined small-size threshold during [a] predetermined time period** [as claimed].'" Appeal Brief 15. Appellant argues that Ng does not disclose disputed claim limitation because:

> In Ng, "a controller of a storage device identif[ies] the aligned and unaligned portions of received data, temporarily stor[es] the aligned and unaligned portions in different queues, and then writ[es] portions from the unaligned data queue or the aligned data queue in parallel to the non-volatile memory areas when one of the queues has been filled with a threshold amount of data or when the controller detects a timeout condition." (Ng, abstract).

Appeal Brief 15.

We find Appellant's arguments persuasive. The Examiner findings that Ng discloses the disputed limitation is not sufficient. *See* Final Action 3. The Examiner relies upon Ng's paragraphs 19 and 22, but instead of reciting or indicating any specific teachings within the paragraphs, the Examiner instead relies upon the entirety of the cited paragraphs. *See* Final Action 3. Upon review of the Ng's paragraphs 19 and 22, we find the paragraphs are silent in regard to disclosing "determining whether the region has a history of I/O requests to access data, in the region in the logical address space of the host, of size less than a predefined small-size threshold during a predetermined time period" as recited in claim 1. The Examiner proffered more explanation of the findings in the Answer, citing to other Ng paragraphs in an attempt to support the combination of references; however, we find the explanation falls short of establishing that Ng teaches or suggests the disputed claim limitation. *See* Answer 24–25. "It is

impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *See In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (citations omitted).

The Examiner relied upon Edmondson to disclose that coalescing multiple write operations into a single write operation is well known in the art. *See* Final Action 4 (*citing* Edmondson column 2, lines 1–29 ("Coalescing multiple write operations into a single write operation improves performance, because it avoids the read-modify-write operations that would otherwise be needed.")). However, the Examiner does not show that Edmondson teaches or suggests "determining whether the region has a history of I/O requests to access data, in the region in the logical address space of the host, of size less than a predefined small-size threshold during a predetermined time period," as recited in claim 1. Accordingly, we find that not only does Ng fail to address Simionescu's noted deficiency, we also find that Edmondson fails to address the deficiencies of the Simionescu and Ng combination. Therefore, obviousness has not been established. *See* Final Action 3–4. We reverse the Examiner's obviousness rejection of independent claim 1, as well as, the obviousness rejection of independent claims 15, 19 and 20 all commensurate in scope with claim 1. Accordingly, we also reverse the Examiner's obviousness rejections of claims 2–14, 16–18 and 21–23 dependent upon claims 1, 15, 19 and 20.

CONCLUSION

Claims Rejected	35 U.S.C. §	References	Affirmed	Reversed
1, 3–8, 10–12, 15, 17, 19, 20, 22	103	Simionescu, Ng, Edmondson		1, 3–8, 10–12, 15, 17, 19, 20, 22
2, 16, 21	103	Simionescu, Ng, Edmondson, Palmer		2, 16, 21
9, 18, 23	103	Simionescu, Ng, Edmondson, Udayashankar		9, 18, 23
13, 14	103	Simionescu, Ng, Edmondson, Fleischer		13, 14

REVERSED