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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte XIAOWEI DENG, WAH KIT LOH,
ANAND SESHARDI, and ZHONGHAI SHI

Appeal 2018-003597
Application 14/083,637
Technology Center 2800

BEFORE BEVERLY A. FRANKLIN, MICHAEL P. COLAIANNI, and MICHAEL G. McMANUS, *Administrative Patent Judges*.

McMANUS, *Administrative Patent Judge*.

DECISION ON APPEAL

Pursuant to 35 U.S.C. § 134(a), Appellant[1] seeks review of the Examiner's decision to reject claims 1–20. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42. Appellant identifies the real party in interest as Texas Instruments Incorporated. Appeal Brief filed Feb. 2. 2016 ("Appeal Br.") 3.

CLAIMED SUBJECT MATTER

The present application generally relates to integrated circuits, such as those employed in solid-state memory. Specification filed Nov. 19, 2013 ("Spec.") ¶ 3. The application further relates to static random access memory (SRAM) cells and devices. *Id.* SRAM memory is taught to be useful because data stored in an SRAM cell remains static so long as power is applied to the memory. *Id.* 4. This is in contrast to "dynamic" RAM ("DRAM"), in which the data must be periodically refreshed in order to be retained. *Id.*

One type of SRAM cell known in the art is an 8 transistor ("8-T") SRAM cell. *Id.* ¶ 19. Figure 1b, reproduced below, depicts an 8 transistor SRAM cell.

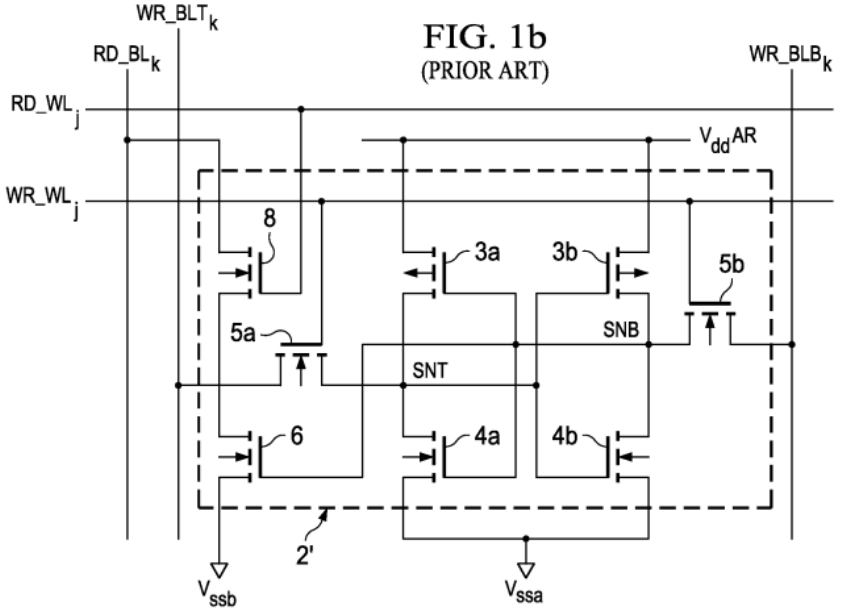

FIG. 1b
(PRIOR ART)

Figure 1b illustrates an 8 transistor SRAM cell that includes a "read buffer constructed of n-channel MOS transistors 6, 8" shown on the left side of the figure. *Id.* ¶ 19. The Specification further teaches that "buffer transistors 6,

8 are generally constructed to be much larger (*i.e.*, with relatively large channel widths) than latch transistors 3, 4, and pass transistors 5." *Id.* ¶ 20.

The incorporation of large buffer transistors adjacent to smaller transistors can give rise to "proximity effects and cross-diffusion effects." *Id.* ¶ 21. This may result in an undesirable imbalance in the operation of the latch portion of the cells. *Id.* This effect is taught to be more pronounced in memory cells with "deep sub-micron transistor sizes." *Id.*

The Specification teaches that the transistors nearer the large buffer transistor "are constructed to have different physical characteristics relative to counterpart transistors in that cell, to compensate for the effect of the asymmetric feature [*i.e.*, read buffer] on the transistor electrical characteristics in the nearer inverter." *Id.* ¶ 28; *see also id.* ¶ 47.

Claim 1 is illustrative of the subject matter on appeal and is reproduced below with certain limitations bolded for emphasis:

> 1. A memory cell formed in a contiguous bit cell area of an integrated circuit, comprising:
>
> a first inverter comprised of a first transistor, the first inverter having an output at a first storage node and an input coupled to a second storage node;
>
> a second inverter comprised of a second transistor, the second inverter having an output at the second storage node and an input coupled to the first storage node, the second transistor serving a circuit function in the second inverter that is the same as the circuit function served by the first transistor in the first inverter; and
>
> a buffer circuit disposed within the bit cell area nearer to the first inverter than to the second inverter;
>
> **wherein the first transistor has a physical construction different from the second transistor**.

Appeal Br. 78 (Claims App.) (emphasis added).

REFERENCES

The Examiner relies upon the following prior art:

Name	Reference	Date
Arsovski	US 2008/0219096 A1	Sept. 11, 2008
Takeda	JP 2006-269023A	Oct. 5, 2006
Chang	Chang et al., *An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches*, 43 IEEE Journal of Solid-State Circuits, 956 (April 2008)	April 2008
Applicant Admitted Prior Art ("AAPA")	Specification, Figure 1b	

REJECTIONS

The Examiner maintains the following rejections:

1. Claims 1–8 and 12–17 are rejected under 35 U.S.C. § 103(a) (pre-AIA) as unpatentable over Arsovski in view of Chang and further in view of the Applicant Admitted Prior Art. Final Act. 4–21.[2]
2. Claims 9–11 and 18–20 are rejected under 35 U.S.C. § 103(a) (pre-AIA) as unpatentable over Arsovski in view of Chang, AAPA, and further in view of Takeda. *Id.* at 21–24.

[2] Claim 6 is omitted from the rejection heading but is discussed in the body of the rejection. Final Act. 4–5, 18–19. Claim 6 is further included in the list of "Maintained Rejections" set forth in the Answer. Answer 2. Accordingly, we consider Rejection 1 to be applicable to claim 6.

DISCUSSION

Rejection 1. The Examiner rejects claims 1–8 and 12–17 as obvious over Arsovski in view of Chang and further in view of the AAPA. *Id.* at 4–21. We address the rejection of claim 1 first.

Claim 1

The Examiner relies on Arsovski as teaching a first transistor that "has a physical construction different from the second transistor." *Id.* at 6.

Arsovski is titled "DEVICE THRESHOLD CALIBRATION THROUGH STATE DEPENDENT BURNIN." Arsovski, code (54). It "relates to a method of compensating for process-induced Random Device Variation (RDV)" in circuitry. *Id.* ¶ 2. Arsovski teaches that, as devices such as field effect transistors shrink in size, "threshold voltage variations between transistors formed on the same wafer have increased, for example, due to variations in dopant concentrations." *Id.* ¶ 29.

Arsovski further teaches as follows:

> [S]emiconductor memory arrays, such as static random access memory arrays (SRAMs), incorporate memory cells with cross-coupled transistors that require a balanced state to effectively store data and sense-amplifiers (SA) with cross-coupled transistors that require a balanced state to effectively detect small voltage signals on largely capacitive array lines. Mismatches between the cross-coupled transistors (i.e., variations in threshold voltage, length, width, and other device parameters between the cross-coupled transistors) in both the individual memory cells and the sense-amplifiers can produce incorrect results.

Id. ¶ 4. Arsovski teaches to prevent mismatches by "initiating a burn-in process during which individually selected states are applied to each of the

devices in the circuit." *Id.* ¶ 33. Arsovski teaches that "[t]his fatigues those devices away from their preferred states and towards a balanced state." *Id.* That is, Arsovski teaches that transistors tend to have different characteristics due to random variation arising during manufacture. Arsovski teaches a process to "fatigue" the transistors so that they achieve a balanced state. *Id.*

The Examiner cites to Figure 8 of Arsovski, reproduced below, in support of the finding that Arsovski teaches transistors with different "physical construction." Final Act. 6.

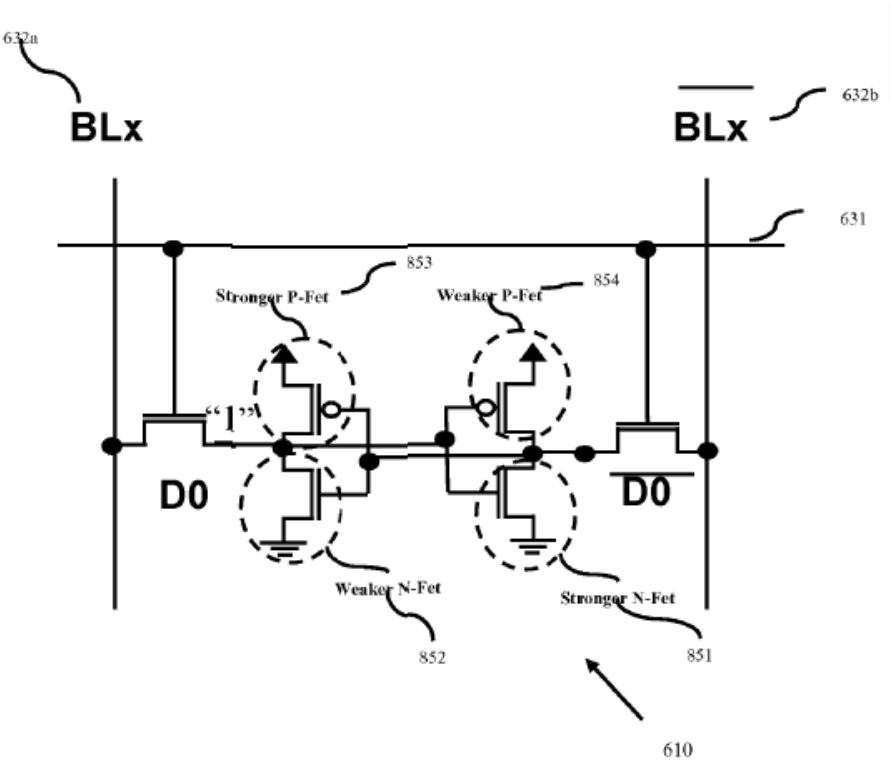

Figure 8 shows an exemplary memory cell. Arsovski ¶ 25. The figure indicates that transistor 851 is the "Stronger N-Fet" while transistor 852 is the "Weaker N-Fet." *Id.*, Fig. 8; *see also id.* ¶ 48. The Examiner identifies transistor 852 as the claimed "first transistor" and transistor 851 as the "second transistor." Final Act. 6.

Appellant argues that Arsovski does not teach that the first transistor has a physical construction different from the second transistor. Appeal Br. 16–20. Rather, Appellant argues that Arsovski concerns random variation while the Specification teaches that the transistor characteristics are intentionally different. A portion of Appellant's argument is set forth below.

> The Appellant[] submit[s] Arsovski et al. teaches that "variations in threshold voltage, length, width, and other device parameters between cross-coupled transistors" (paragraph 0004) are caused by "process induced Random Device Variation (RDV)" (paragraph 0002) as "technology scales to sub-micron geometries" (paragraph 0003). Therefore, the RDV taught by Arsovski et al. is comparable to the "proximity effects" taught in the [Appellant's] Specification (e.g.[,] paragraphs 0012-0018, 0042). In paragraph 0029 of Arsovski et al. (that is cited on page 6 of the Office Action) the RDV is described as problematic because it "can limit the performance and/or reliability of circuits that incorporate such transistors." The **Appellant[ ] teach[es] the opposite of Arsovski et al. by teaching the implementation of an intentional difference in "physical construction"** (Claim 1 and paragraph 0047) of memory cells "to compensate for these proximity effects" (paragraph 0043) "during design of the integrated circuit layout or its manufacturing process flow" (paragraph 0047).

Appeal Br. 17 (emphasis added). Thus, Appellant argues that the random variation between the two transistors of Arsovski (e.g., the stronger and weaker N-FETs) differs from a first transistor with a "physical construction different from" a second transistor as required by claim 1.

Appellant argues that the following portion of the Specification defines the term "physical construction":

> According to embodiments of this invention, one or more of load transistor 33a, driver transistor 34a, and pass transistor 35a . . . is constructed to have different drive strength than its

> counterpart load transistor 33b, driver transistor 34b, and pass transistor 35b, respectively. **This difference in construction** between these typically matched transistors **is selected, during design of the integrated circuit layout or its manufacturing process flow**, to compensate for the proximity effects exerted by transistors 36, 38 in cell 30. As a result . . . the proximity effects caused by buffer transistors 36, 38 on one side of cell 30 (but not on the other) result in cell 30 becoming electrically balanced, and exhibiting the corresponding cell stability.

Spec. ¶ 47 (emphasis added).

Thus, Appellant argues that "physical construction different from" should be construed to mean a "physical construction *intentionally* different from." We do not adopt Appellant's proposed claim construction. Structural claims, such as claims directed to an article or apparatus, must be distinguished from the prior art in terms of structure. *See In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997) (and cases cited therein); *see also In re Danly*, 263 F.2d 844, 848 (CCPA 1959) ("Claims drawn to an apparatus must distinguish from the prior art in terms of structure rather than function.").

Appellant's proposed construction (requiring an intentional difference in physical manufacture) would require that the limitation at issue be construed as a product-by-process limitation (a limitation that defines a product in terms of the process used to make the product). Even such construction, however, would not impart patentability if the prior art teaches the claimed structural features. *See, e.g.*, *SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312, 1315 (Fed. Cir. 2006) ("[O]nce a product is fully disclosed in the art, future claims to that same product are precluded, even if that product is claimed as made by a new process.").

Appellant further argues that dependent claim 9 supports its position. Appeal Br. 19. Claim 9 depends from claim 1 and further requires that "the first and second transistors differ from one another in construction by one or more attributes selected from the group consisting of channel width, channel length, and net channel dopant concentration." *Id.* at 82 (Claims App.). Appellant argues that "under the doctrine of claim differentiation the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." *Id.* at 19. Appellant further argues that, therefore, "differences in physical construction" "include one or more of the attributes listed in dependent Claim 9 of channel width, channel length, and net channel dopant concentration." *Id.*

The Patent Act provides that "a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed." 35 U.S.C. § 112(d). "Claims of narrower scope can be useful to clarify the meaning of broader, independent claims under the doctrine of claim differentiation." *In re Tanaka*, 640 F.3d 1246, 1250 (Fed. Cir. 2011) (citation omitted). That is, an independent claim must be broad enough in scope to encompass the limitation enumerated in the dependent claim. Accordingly, the differences listed in claim 9, such as dopant concentration, fall within the scope of "differences in physical construction." This does not, however, bear upon whether such differences must be intentionally selected.

Appellant additionally argues that "the RDV taught by Arsovski et al. is comparable to the 'proximity effects' taught in the Appellant['s] Specification." Appeal Br. 17. This is inadequately supported. Arsovski

describes random device variation as "process-induced" (Arsovski ¶ 2), that is, arising during manufacture. Proximity effects result from larger buffer circuits being located near smaller pass and driver transistors. Spec. ¶ 20–21. Appellant fails to show how these separate effects are "comparable."

Appellant further argues that Arsovski teaches away from the claimed invention by teaching that it is calibrated after manufacture. Appeal Br. 17. Appellant additionally argues that Arsovski teaches away from a difference in physical construction by teaching that "mismatches" between the cross-coupled transistors can produce incorrect results (citing Arsovski ¶ 4) and further teaches that "[t]he present invention takes advantage of this observation and comprises a method embodiments [sic] for reducing and/or eliminating mismatch" (*id.* ¶ 32).

Prior art may teach away if it "criticize[s], discredit[s], or otherwise discourage[s] the solution claimed." *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Teaching away requires "clear discouragement" from implementing a technical feature. *In re Ethicon, Inc.*, 844 F.3d 1344, 1351 (Fed. Cir. 2017).

Here, Arsovski teaches a method to tune mismatched transistors so that they achieve a balanced state. Arsovski ¶ 4. Arsovski teaches that one of the physical differences that may lead to mismatch is "variations in dopant concentrations." *Id.* Variation between two transistors in dopant concentration is a difference in physical construction. *See* Appeal Br. 82 (claim 9). Appellant does not cite to any teaching that such difference would be changed by Arsovski's burn-in process. Rather, the transistor(s) would be calibrated to achieve a balanced state despite such physical difference. *See* Answer 5–6. Nor does Arsovski teach that random device

variation is an option that one may avoid at will. Accordingly, Arsovski does not teach away from the use of transistors having physical differences; it teaches how to use such transistors to achieve a balanced circuit.

In view of the foregoing, Appellant has not shown error in the rejection of claim 1.

Claim 2

Appellant also alleges error in the rejection of dependent claim 2. Appeal Br. 21–23. Claim 2 depends from claim 1 and further requires that "the first transistor is disposed in the bit cell area of the memory cell between the buffer circuit and the second transistor." *Id.* at 78 (Claims App.). First, Appellant repeats its argument that Arsovski "teaches away from the claimed invention of a first transistor having a physical construction different from the second transistor." *Id.* at 21–22. This argument is not persuasive for the reasons set forth above.

Appellant further argues that Chang does not teach that the first transistor is disposed between the buffer circuit and the second transistor. *Id.* In the Answer, the Examiner presents an annotated version of Chang's Figure 2(b) showing a grouping of three transistors labeled "T1 [transistor 1] is one of these (e.g., D2)." Answer 9. Appellant's opening brief does not address such point and Appellant did not file a Reply Brief. Accordingly, we determine that Appellant has not rebutted the Examiner's finding set forth in the Answer.

Appellant additionally argues that Chang teaches that there are no differences in physical construction between the first and second transistors.

Appeal Br. 22. The Examiner, however, does not rely on Chang as teaching such differences. *See* Answer 10.

Appellant also briefly argues that Chang teaches away from such differences "by teaching that there are no differences in physical construction between the first and second transistors." Appeal Br. 22. This is not persuasive – "mere disclosure of alternative designs does not teach away." *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

Appellant argues that the AAPA does not teach the elements of claim 2 because it does not teach a first transistor disposed between the buffer circuit and the second transistor in addition to transistors having different physical construction. Appeal Br. 22. The Examiner cites element 4a of Figure 1b of the Specification (labeled "PRIOR ART") as teaching a first transistor between the buffer and the second transistor. Final Act. 15; Answer 10. Appellant does not specifically rebut this finding. Further, the Examiner primarily relies on Arsovski as teaching the claimed physical differences, *see* above. Final Act. 6.

Appellant then concludes as follows:

> Neither Arsovski et al., Chang et al., nor the AAPA teach that the first transistor has a physical construction different from the second transistor; therefore, the combination of those references also does not teach that the first transistor has a physical construction different from the second transistor as required by the combination of Claims 1 and 2.

Appeal Br. 23. Appellant, however, does not address the Examiner's proposed combination *as a whole*. A finding of obviousness cannot be overcome "by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800

F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

In view of all of the foregoing, Appellant has not shown error in the rejection of claim 2.

Claim 3

Appellant also alleges error in the rejection of dependent claim 3. Appeal Br. 23–26. Claim 3 depends from claim 1 and further includes certain limitations regarding the first inverter, the second inverter, and correspondence between the transistors. Appeal Br. 79 (Claims App.).

Appellant does not specifically address any limitation of claim 3 in its briefing. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 4

Appellant also alleges error in the rejection of dependent claim 3. Appeal Br. 26–28. Claim 4 depends from claim 1 and further includes certain limitations regarding the first inverter, the second inverter, and correspondence between the transistors. Appeal Br. 80 (Claims App.). Claim 4 differs from claim 3 in that it includes limitations regarding circuit connectivity. *Id.*

Appellant does not specifically address any limitation of claim 4 in its briefing. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 5

Appellant also alleges error in the rejection of dependent claim 5. Appeal Br. 29–31. Claim 5 depends from claim 4 and further requires that "the first driver transistor also has a physical construction different from the second driver transistor." *Id.* at 80 (Claims App.).

Appellant does not specifically address any limitation of claim 5 in its briefing. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 6

Appellant also alleges error in the rejection of dependent claim 6. Appeal Br. 31–33. Claim 6 depends from claim 1 and further requires two pass transistors of different physical construction. *Id.* at 81 (Claims App.).

Appellant does not specifically address any limitation of claim 6 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 7

Appellant also alleges error in the rejection of dependent claim 7. Appeal Br. 34–36. Claim 7 depends from claim 1 and further requires, *inter alia*, a buffer having feature sizes larger than the corresponding feature sizes of the first and second transistors. *Id.* at 81 (Claims App.).

Appellant does not specifically address any limitation of claim 7 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 8

Appellant also alleges error in the rejection of dependent claim 8. Appeal Br. 37–39. Claim 8 depends from claim 7 and further requires that "the gate of the second buffer transistor is connected to the second storage node." *Id.* at 81 (Claims App.).

Appellant does not specifically address any limitation of claim 7 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 12

Appellant also alleges error in the rejection of independent claim 12. Appeal Br. 39–44. Claim 12, although more narrow in scope, is generally similar to claim 1. *Id.* at 78, 83–84. (Claims App.). Appellant sets forth the same arguments in regard to claim 12 as presented with regard to the rejection of claim 1. *Compare id.* at 16–20 with 39–44. These arguments are not persuasive of error for the reasons set forth in regard to claim 1, *supra*.

Claim 13

Appellant also alleges error in the rejection of dependent claim 13. Appeal Br. 44–46. Claim 13 depends from claim 12 and further includes certain limitations regarding the location of the first and second transistors. *Id.* at 85 (Claims App.).

Appellant does not specifically address any limitation of claim 13 in its briefing in more than a summary manner. Indeed, Appellant describes only a portion of the limitation in its briefing. *Id.* at 44. In support of its allegation of error Appellant repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 14

Appellant also alleges error in the rejection of dependent claim 14. Appeal Br. 46–49. Claim 14 depends from claim 12 and further includes certain limitations regarding the first inverter, the second inverter, and correspondence between the transistors. *Id.* at 85 (Claims App.).

Appellant does not specifically address any limitation of claim 14 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 15

Appellant also alleges error in the rejection of dependent claim 15. Appeal Br. 49–52. Claim 15 depends from claim 12 and further includes certain limitations regarding the first load and drive transistors, the second

inverter, and correspondence between the transistors. *Id.* at 86 (Claims App.).

Appellant does not specifically address any limitation of claim 15 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 16

Appellant also alleges error in the rejection of dependent claim 16. Appeal Br. 52–54. Claim 16 depends from claim 15 and further requires that "the first driver transistor also has a physical construction different from the second driver transistor." *Id.* at 86 (Claims App.).

Appellant does not specifically address any limitation of claim 16 beyond those arguments presented in regard to claim 2. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

Claim 17

Appellant also alleges error in the rejection of dependent claim 17. Appeal Br. 54–56. Claim 17 depends from claim 12 and further requires that "the first pass transistor also has a physical construction different from the second pass transistor." *Id.* at 86 (Claims App.).

Appellant does not specifically address any limitation of claim 17 beyond those arguments presented in regard to claim 2. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 2. This is not persuasive of error for the reasons set forth in regard to claim 2.

In view of the foregoing, Appellant has not shown error in the rejection of claims 1–8 and 12–16 as obvious over Arsovski, Chang, and the Applicant Admitted Prior Art.

Rejection 2. The Examiner rejects claims 9–11 and 18–20 as obvious over Arsovski, Chang, the Applicant Admitted Prior Art, and Takeda. Final Act. 21–24. Appellant argues for the reversal of this rejection as to each claim at issue. Appeal Br. 57–76. We consider each claim in sequence.

Claim 9

Appellant alleges error in the rejection of claim 9. Appeal Br. 57–60. Claim 9 depends from claim 1 and further requires that "the first and second transistors differ from one another in construction by one or more attributes selected from the group consisting of channel width, channel length, and net channel dopant concentration." *Id.* at 82 (Claims App.). In support of its allegation of error, Appellant repeats arguments set forth in support of its appeal of the rejection of claims 1 and 2. *See id.* at 17–18, 21–23. We determine these arguments not to be persuasive for the reasons set forth above.

In addition, Appellant argues that Takeda "does not teach that the first and second transistors differ from one another in construction by one or more attributes selected from the group consisting of channel width, channel length, and net channel dopant concentration for a memory cell having a buffer circuit." *Id.* at 60.

In the Final Action, the Examiner finds that "Takeda teaches reducing the drive capability of one of the drive transistors (e.g., Fig. 4: N2) so as to increase the threshold voltage (see para. 0039)." Final Act. 22. The Examiner further finds that "Takeda specifically teaches that the drive strength can be reduced by, *notably*, increasing the channel length, decreasing the channel width, or increasing the dopant concentration (see para. 0039)." *Id.*

In the Answer, the Examiner indicates that "Takeda was relied upon to supplement Arsovski's explanation of the physical differences and highlight how to improve the operating characteristics by variously increasing or decreasing the channel length, channel width, and dopant concentration of one of the transistors (see Final Act. 21-23; see esp. Takeda para. 0039)." Answer 19.

Appellant does not specifically address these findings. Accordingly, Appellant has not shown error in the Examiner's findings regarding Takeda. *See* 37 C.F.R. § 41.37(c)(1)(iv).

Additionally, Appellant does not address the Examiner's proposed combination as a whole. *See* Appeal Br. 60. As above, a finding of obviousness cannot be overcome "by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d at 1091.

In view of the foregoing, Appellant has not shown error in the rejection of claim 9.

Claim 10

Appellant also alleges error in the rejection of claim 10. Appeal Br. 61–63. Claim 10 depends from claim 9 and further requires that the buffer circuit reduces the source/drain strength of the first transistor and that the buffer circuit is constructed to have one or more of "a larger channel width, a shorter channel length, and a lower net channel dopant concentration." *Id.* at 82 (Claims App.).

Appellant does not specifically address any limitation of claim 10 in its briefing in more than a summary manner. Rather, it repeats, substantially verbatim, its briefing set forth in regard to claim 9 (omitting the argument regarding random device variation found on page 58). Compare *id.* 58–60 (regarding claim 9) *with* 61–63 (regarding claim 10). This is not persuasive of error for the reasons set forth in regard to claim 9.

Claim 11

Appellant also alleges error in the rejection of claim 11. Appeal Br. 64–66. Claim 11 depends from claim 9 and further requires that the buffer circuit increases the source/drain strength of the first transistor and the first transistor is constructed to have one of "a *smaller* channel width, a *longer* channel length, and a *higher* net channel dopant concentration." *Id.* at 82 (Claims App.) (emphasis added).

Appellant asserts that claim 10 specifies that "the first transistor is constructed to have, relative to the second transistor, one or more of the attributes selected from the group consisting of a *larger* channel width, a *shorter* channel length, and a *lower* net channel dopant concentration." *Id.* at 64 (emphasis added). That is, Appellant appears to have conflated certain

limitations of claims 10 and 11. Appellant then presents the same argument, substantially verbatim, for claim 11 as for claim 10, despite the inversion of the limitations between the two claims. This is also the briefing submitted in regard to claim 9. *Compare id.* at 57–60 *with* 64–66. For the reasons set forth with regard to claim 9, we do not find such arguments to be persuasive.

Claim 18

Appellant also alleges error in the rejection of claim 18. Appeal Br. 67–70. Claim 18 depends from claim 12 and further requires that the first and second transistors of each cell differ from one another in one of "channel width, channel length, and net channel dopant concentration." *Id.* at 87 (Claims App.).

Claim 18 (which depends from claim 12) includes limitations similar to claim 9 (which depends from claim 1). *Id.* at 82, 87. Appellant presents the same argument for claim 18 as for claim 9. *Compare id.* at 57–60 *with* 67–70. For the reason set forth above with regard to claim 9, we do not find such arguments to be persuasive.

Claim 19

Appellant also alleges error in the rejection of claim 19. Appeal Br. 70–73. Claim 19 depends from claim 18 and further requires that the buffer circuit reduces source/drive strength of the first transistor and have one of "larger channel width, a shorter channel length, and a lower net channel dopant concentration." *Id.* at 87 (Claims App.).

Appellant does not specifically address any limitation of claim 19 in its briefing in more than a summary manner. Rather, it repeats, substantially

verbatim, its briefing set forth in regard to claim 9 (omitting the argument regarding random device variation found on page 58). *Compare id.* 58–60 (regarding claim 9) *with* 70–73 (regarding claim 19). This is not persuasive of error for the reasons set forth in regard to claim 9.

Claim 20

Appellant also alleges error in the rejection of claim 20. Appeal Br. 73–76. Claim 20 depends from claim 18 and further requires that the buffer circuit *increases* the source/drain strength of the first transistor and the first transistor is constructed to have one of "a *smaller* channel width, a *longer* channel length, and a *higher* net channel dopant concentration." *Id.* at 87 (Claims App.) (emphasis added).

Appellant asserts that claim 20 specifies that "the first transistor is constructed to have, relative to the second transistor, one or more of the attributes selected from the group consisting of a *larger* channel width, a *shorter* channel length, and a *lower* net channel dopant concentration." *Id.* at 74 (emphasis added). That is, Appellant appears to have conflated certain limitations of claims 19 and 20. Appellant then presents the same argument, substantially verbatim, for claim 20 as for claim 19, despite the inversion of the limitations between the two claims. This is further duplicative of the briefing submitted in regard to claim 9. *Compare id.* at 57–60 *with* 73–76. For the reasons set forth with regard to claim 9, including failure to present argument addressed to the Examiner's proposed combination as a whole, we find such arguments to be unpersuasive.

CONCLUSION

The Examiner's rejection of claims 1–8 and 12–17 as obvious over Arsovski, Chang, and AAPA is affirmed. The Examiner's rejection of claims 9–11 and 18–20 as obvious over Arsovski, Chang, AAPA, and Takeda is affirmed.

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–8, 12–17	103(a)	Arsovski, Chang, AAPA	1–8, 12–17	
9–11, 18–20	103(a)	Arsovski, Chang, AAPA, Takeda	9–11, 18–20	
Overall Outcome			1–20	

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED